VI. Multiple-Mission Telemetry System

A. Introduction, *W. S. Baumgartner*

The Jet Propulsion Laboratory has been recovering telemetry from space vehicles for ten years. Over this period, wide ranges of subcarrier frequencies, data rates, and types of modulation have been used. Each project has selected parameters for its telemetry requirements, and, because each was different, the ground demodulation equipment has differed. This has necessitated equipping ground stations assigned to a particular mission with "mission-dependent" demodulation equipment which has varied from 5 to 20 racks per station. While providing maximum design freedom, this system was costly in equipment, installation time, and training time. It also limited DSN flexibility, since only stations having the mission-dependent equipment could support that mission.

The *Mariner IV*, *Pioneer*, *Lunar Orbiter*, *Apollo*, *Mariner* Venus 67, *Mariner* Mars 1969, and *Voyager* spacecraft use, or will use, PCM-PM-PM[1] as the telemetry mode. Therefore, this mode is evolving into a standard for deep space communications. This project recognizes this mode of telemetry transmission as a standard and provides general-purpose mission-independent equipment capable of meeting the requirements of all these projects at each DSN station. The universal nature of this equipment makes it a long-term installation to handle engineering and medium rate science telemetry.

The multiple mission telemetry system (MMTS) consists of a subcarrier demodulation loop which accepts 10-MHz signals from the receiver, phase-modulated with one or more square wave subcarriers which, in turn, are phase-modulated with data. The demodulation is accomplished in a manner which does not lose the power in the square wave harmonics. Bit synchronization is accomplished in a computer operating in conjunction with special-purpose digital equipment by using the transitions in the telemetry data stream. To change from one spacecraft to another, it is only necessary to change the computer program and reset the subcarrier VCO, certain bandwidths, and time constants. Ultimately, this will all be accomplished from the computer program.

[1]Pulse code modulated–phase modulated–phase modulated.

A separate channel for subcarrier and bit synchronization is not required from the spacecraft; therefore, this power may be used to increase the power in the information channels. A fixed-phase relationship between subcarrier and bit timing is no longer required. This removes the requirement for rigid bit timing in the various spacecraft data sources and results in simplification of the spacecraft subsystem interfaces. This simplification of spacecraft electronics is expected to increase reliability.

As an additional feature the system also includes dual back-up data recordings for recovery of data in the event of equipment malfunction. Each multiple mission telemetry system can handle one subcarrier. Two systems will be installed at each station, but dual channel operation will be possible only if two computers are available. The entire system will consist of two racks installed with the receiver exciter subsystem housing two subcarrier demodulators and two racks installed with the telemetry and command processor housing digital equipment. The existing SDS 920 computers will be used. One additional rack of signal simulation or test equipment will be provided to each station.

As originally installed, the system will handle the following signals:

Function	Subcarrier	Data rate
Engineering telemetry	20 to 40 kHz	8 to 512 bits/s
Nonvideo science data	40 to 80 kHz	32 to 512 bits/s

These boundaries have been chosen to meet operating and design requirements. By keeping all subcarriers higher than 20 kHz the problem of carrier loop acquisition is simplified. The upper limit of 512 bits/s represents 66% utilization of the SDS 920 computer for bit synchronization, detection, and signal-to-noise computation. The lower limit of 8 bits/s on engineering telemetry represents the lowest bit rate at which adequate predetection bandwidths can be achieved at the standard IF frequency. There is an additional constraint at low data rates related to loop bandwidth versus dynamic capability. The lower limit of 32 bits/s on nonvideo science data represents the lowest bit rate at which the required loop bandwidth can accommodate the doppler on an 80-kHz subcarrier.

In addition to the above requirements, the subcarrier demodulation loop only is designed to handle video science data at subcarriers of 80 to 1000 kHz and rates of 512 bits to 100 kbits/s. This is to provide additional capacity for future high rate requirements. There is an additional consideration to be observed in selecting subcarriers. Exact subharmonics of the 10-MHz intermediate frequency (such as 1000, 100, 50 kHz, etc.) should be avoided. A low bit-rate option, not scheduled for installation at this time, will provide for bit rates down to 1 bit/s.

The first project to use the new system will be *Mariner* Mars 1969. To support this project, a DSN readiness date of September 1, 1968 has been established. By this date, five stations will be equipped, checked out, and operational. The first complete system will be delivered to the Flight Project/Tracking and Data Acquisition Interface Laboratory at JPL in February, 1968 for use in spacecraft check-out.

This article will present a complete system description, a set of specifications, a system analysis, equipment and software descriptions, and results of preliminary tests to date. Future articles will report any design modifications.

B. System Description, *W. Frey*

1. Equipment Functional Description

Figure 1 shows a functional block diagram of the (MMTS) equipment as it will be implemented into the DSIF. The system consists of three major hardware elements: (1) Subcarrier demodulator assembly (SDA), which tracks the received subcarrier and extracts the telemetry data stream from the subcarrier and 10-MHz carrier input from the receiver-exciter (RE) subsystem. The subcarrier demodulator assembly will form a part of the existing (RE) subsystem when it is implemented into the DSIF. (2) Computer and peripheral digital equipment assembly which accepts the data stream output from the subcarrier demodulator assembly and: (a) generates a clock at the data rate frequency and in phase with the telemetry data transitions (bit synchronization), (b) detects the telemetry data bits at each data clock time (bit detection), (c) searches for telemetry data frame synchronization, and (d) decommutates, formats, and outputs the telemetry data in real-time to the ground communications system (GCS) for transmission to the SFOF for further processing and evaluation. The computer and peripheral digital equipment will form a part of the telemetry and command data-handling subsystem (TCD) when it is implemented into the DSIF and will be known as the telemetry and command processor (TCP) Phase II-C configuration. (3) A rack of test equipment which provides test signals which are used to evaluate the performance of the MMTS.

Detailed functional descriptions of each of the three major hardware elements follow.

a. Subcarrier demodulator assembly. The subcarrier demodulator assembly receives an input from the RE subsystem of a 10-MHz carrier frequency which is phase-modulated by a square wave subcarrier and binary telemetry data generated in the spacecraft. The output of the SDA is an extracted data stream which is sent to the computer and digital equipment for bit synchronization and detection. Figure 1 contains a functional diagram of the SDA. The SDA removes the subcarrier and the 10-MHz IF carrier, in that order, from the input signal to provide the data stream output. The upper portion of the block diagram shows the path of the data stream, and the lower portion is a phase-locked loop which tracks the subcarrier. A local estimate of the data stream is injected in the subcarrier phase-locked loop to remove the modulation by the data on loop phase-error signal.

The input signal (point 1), consisting of 10 MHz modulated with the square wave subcarrier and data plus receiver noise, is applied to two phase switches. When the loop is in lock, the upper phase switch is switched by a square wave that is the local estimate of a subcarrier which is in phase and frequency agreement with the input subcarrier. The lower phase switch is switched by a local subcarrier estimate that is 90 deg out of phase with the input subcarrier. The bandwidth of the phase switches allows the SDA to utilize the power contained in the square wave harmonics of the subcarrier as well as the fundamental. The upper phase switch functions as a 10-MHz amplitude detector when the loop is locked with a 10-MHz output switched 180 deg in phase with the data stream. The lower phase switch functions as a phase detector and provides a signal proportional to loop phase error. This signal is also switched 180 deg in phase with the data.

Since the subcarrier is removed from the input signal first, the predetection filtering bandwidth is required to be only wide enough to pass the data and is centered at 10 MHz. This offers the advantage of relatively narrow band filtering and reduces the possibility of noise overloading of the 10-MHz coherent amplitude detectors, which follow the IF filters.

The upper signal (point 2) is synchronously detected with a 10-MHz reference signal from the RE subsystem which is phase coherent with the 10-MHz telemetry input. The output of this coherent amplitude detector (point 3) is a dc level which is switched plus or minus with the data. This extracted data stream is: (1) amplified, integrated, and sent to the computer equipment for bit synchronization and detection (point 10), and (2) sent to a postdetection filter and limiter (point 11) to provide a local strong signal estimate of the data. The postdetection filter reduces the amount of noise on the data (i.e., optimizes signal-to-noise ratio) at the input to the limiter. The output of the limiter (point 4) is a strong signal switching plus and minus one with the data. The local data estimate modulates the 10-MHz reference (point 5). This signal is then multiplied with the output of the 90 deg shifted predetection filter (point 6) in a 10-MHz coherent amplitude detector. The multiplication removes the effect of the data phase switching on the loop phase-error signal and provides an output (point 7) of a valid S-curve that is proportional to loop phase error over $\pm\pi/2$ rad. This signal is then narrow-band filtered (point 8) to remove undesired frequency terms and noise. The dc loop phase-error signal is used to drive a VCO to correct the frequency and phase of preselected subcarrier frequency on the synthesizer. The output of the VCO–synthesizer provides a signal that is in phase and frequency agreement with input subcarrier frequency from the spacecraft. This local estimate of spacecraft subcarrier is applied to the signal shaper and quadrature generator to provide 0- and 90-deg phase square wave signals to the phase switches.

The dashed lines on the functional block diagram of the SDA represent the option that will be installed at a later date to allow the SDA to handle low data rates (i.e., 1 bit/s to 8 bits/s). This option introduces a lower intermediate carrier frequency of 100 kHz. The new IF allows the use of very narrow band filters to pass the low data rates centered at 100 kHz rather than 10 MHz. The narrow filtering is more practical to achieve at 100 kHz than at 10 MHz. Other than the lower IF filtering, the loop in the low data rate option operates in an identical manner to the higher data rates previously described.

An additional input to the SDA is shown at point 9 in Fig. 1. This is a baseband input consisting of a subcarrier modulated by a data stream. This signal modulates a 10-MHz reference in the up-converter. The output of the up-converter is identical to the normal 10-MHz telemetry receiver output. This input channel is utilized when the SDA is in the backup recording playback mode or testing is performed on the MMTS equipment.

The SDA provides a loop in-and-out-of-lock lamp indicator and a meter displaying lock voltage. These indications assist the operator in loop acquisition and provide

an output to the digital instrumentation subsystem for monitoring purposes.

A detailed equipment description of SDA hardware is contained in Sect. E-1.

b. Computer and digital equipment

General description. The computer and digital equipment accepts an input of the integrated binary telemetry data stream from the subcarrier demodulator assembly. The primary function of this equipment is to perform bit synchronization and bit detection of the telemetry data stream. In addition, data frame synchronization, data decommutation (engineering telemetry only) and formatting of the telemetry data for output are accomplished in real-time by the computer. The following outputs from computer and digital equipment are provided:

(1) Formatted telemetry data to the ground communications system. Data is transmitted in real-time on the high-speed data line and teletype lines to the SFOF for central processing and evaluation.

(2) A digital magnetic tape recording of the formatted telemetry data for back-up in case of ground communications system failure and for historical record.

(3) A teletype output of MMTS status and performance together with selected spacecraft engineering measurements are transmitted to the station monitor equipment.

Figure 1 contains a functional block diagram of the computer and digital equipment. The computer and digital equipment combine operations executed by a program in the computer. The digital hardware is located external to the computer but under the control of the computer software.

Descriptions of the computer and digital equipment functions of input of data, bit detection and synchronization, and data frame synchronization, decommutation, and formatting follow in this section of the report.

Data stream input. In performing the bit synchronization and detection functions, it is required that the computer sample the data stream output of the subcarrier demodulator assembly. To minimize the effects of noise on the data stream, the input waveform is integrated over a bit time interval before it is sampled by the computer. This input of the data into the computer is accomplished by use of: (1) data integrator filter (located in the SDA), (2) an analog-to-digital converter (A/DC), and (3) software operating on the input data in the computer. This combination of hardware and software forms an integrate and dump circuit.

Although, for functional clarity, three A/DCs are shown in Fig. 1, in reality only one A/DC is used. It is commanded to sample at three selected times (early, late, and bit timing) during a telemetry bit time interval. The relationship of the sample times is fixed by the timing generator. Once data is integrated over a bit time interval, a command is generated to sample the A/DC which transforms the integrated input voltage to a positive or negative digital value. The command pulse also at this time generates an interrupt to the computer. The interrupted computer then executes software subroutines which read into the computer the digital value of the voltage from the A/DC.

Since the data integrator is not reset at any time, integration is performed over a period of time with an arbitrary initial value. The effect of the integrator time constant and the initial value of the integrator must be taken into consideration in determining the actual value of the sample taken. This is accomplished by the computer program which reduces current sample by the amount of the previous sample (which has been stored in the computer memory) multiplied by decay on the previous sample caused by the integrator time constant over the integration interval. The result is a value that is a function of only the integration of the change of integrator input voltage from previous sample time to the present time and is independent of the initial value of the integrator.

The early and late time inputs are utilized in the bit synchronization loop, and the bit time input is required for bit detection.

Bit detection. Bit detection is accomplished by the computer program operating on the dumped input of the data stream which is sampled by the bit timing command (point 12). A new value of the data is transferred into the computer at the rate of the transmitted data from the spacecraft. The integration, therefore, is over the bit time interval for each input. The software tests the sign of each dumped data input. If the data is positive, a binary *one* is stored in the data table; conversely, if the data is negative, a binary *zero* is stored in the data table (point 13). In order to optimize the probability of correct detection of the data, the integrate and dump input must

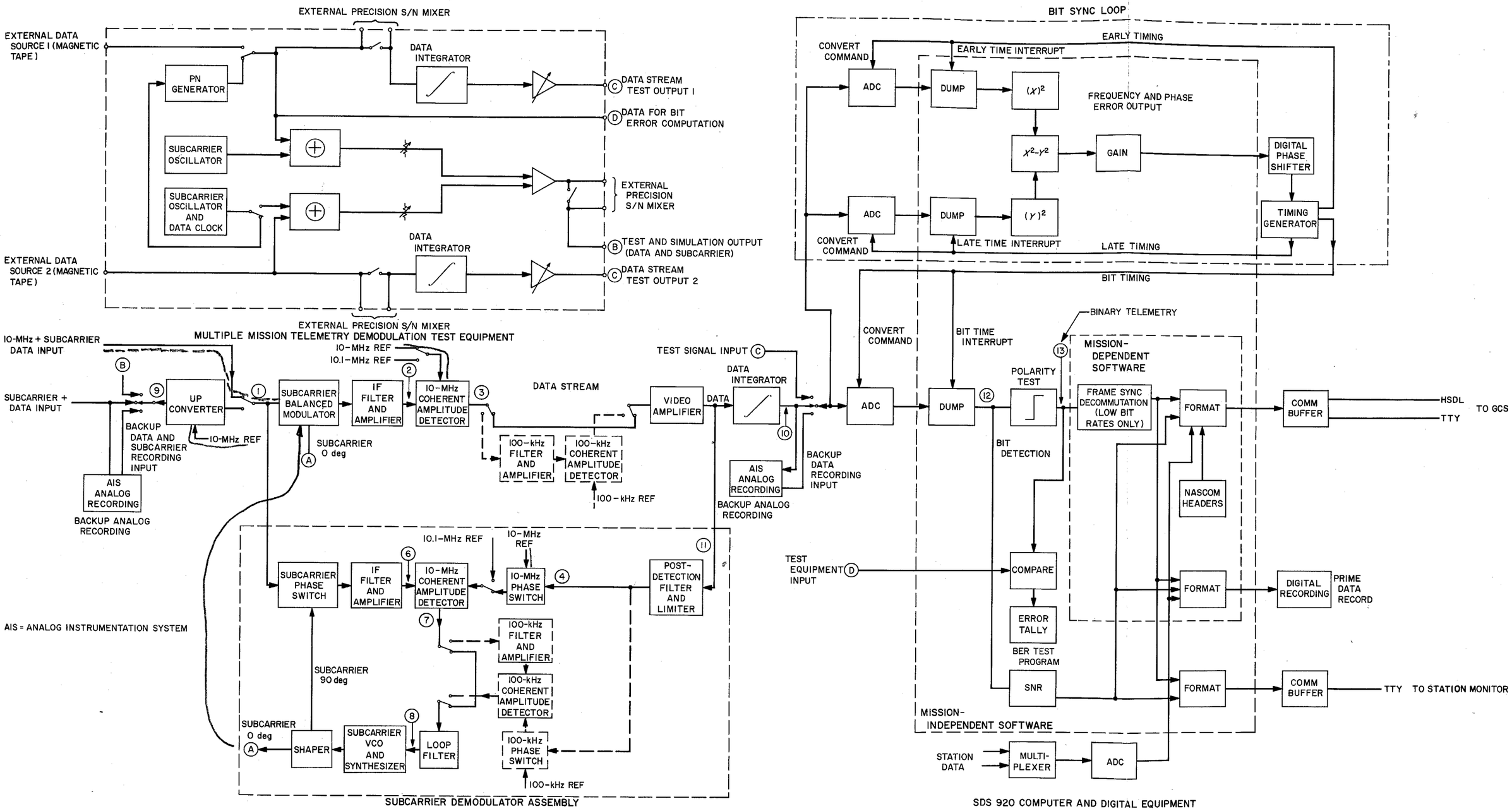


Fig. 1. Multiple-mission telemetry system functional block diagram

10M + TELEM MOD
10M REF
SUB CARR + TELEM
TELEM

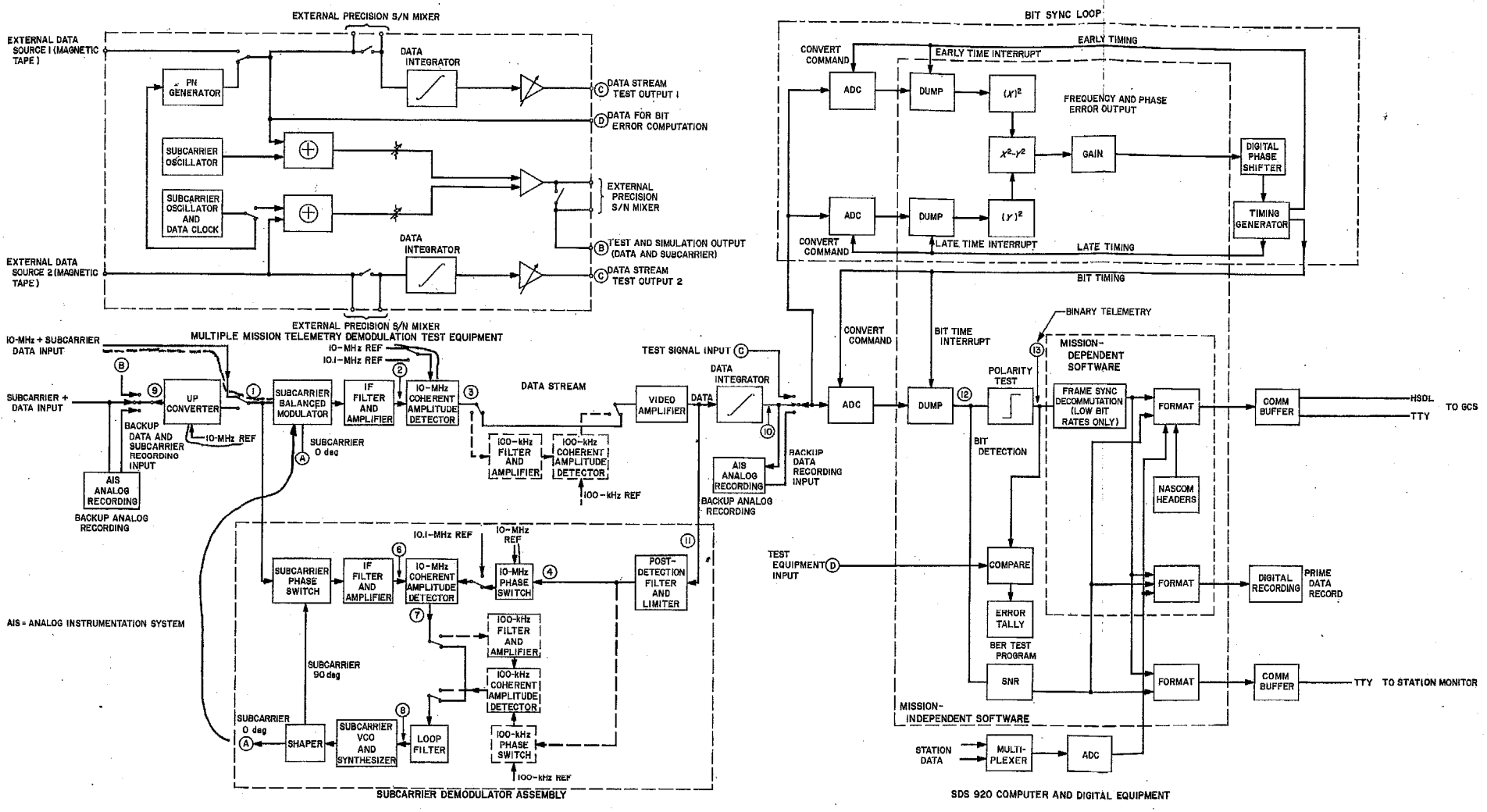


Fig. 1. Multiple-mission telemetry system functional block diagram

10M + TELEM MOD
10 M REF
SUB CARR + TELEM

produce the maximum or minimum value of the integration of each data bit possible under the prevailing signal-to-noise conditions. To accomplish this, the data stream must be sampled at the same frequency that the data is generated in the spacecraft, and it must be in synchronization (phase) with the clock that originates the data in the spacecraft. When this condition occurs, each bit is integrated over the full bit interval without possibility of any data transitions occurring in the interval to reduce the absolute value of the integral. Therefore, the success of the bit detection depends on the frequency and phase of the bit timing command being identical to the data clock in the spacecraft. The bit timing command is produced in the MMTS by the bit synchronization process.

Bit synchronization. The primary function of bit synchronization is to provide the bit detection hardware and software with a clock which is in phase and frequency with the data clock in the spacecraft. Since the spacecraft data clock is not transmitted to the ground stations, the MMTS must construct a local estimate of the spacecraft data clock. The bit synchronization uses a delay lock loop (analyzed in Section C-4) which, based on the transitions in the incoming data stream, tracks the frequency and phase of the spacecraft data clock. Bit synchronization in the MMTS is accomplished by a combination of computer software and external digital equipment which is under control of the software.

The bit synchronization loop operates by: (1) sampling the early and late integrals of the input data stream, (2) squaring the two integrals, (3) differencing the two squares to obtain a phase-error correction signal, (4) controlling the frequency and phase of the digital phase shifter, and (5) generating the early, late, and bit timing commands. (See Fig. 1, bit synchronization loop.)

The early integral is the integration of the input data stream from ¼ of a bit time before the local estimate of the data clock (bit timing command) to ¾ of a bit time after the estimated data clock. The late integral is the integration of the data stream from ¾ of a bit time before the estimated data clock to ¼ of a bit time after the estimated data clock. The sign of the two integrals is removed by squaring to enable the bit sync loop to be independent of both the change of the sign in the integrals due to transitions in the data and the direction of the transitions (i.e., binary 1 to 0 or 0 to 1) in determining phase error. By differencing the squares of the two integrals a loop phase-error signal is obtained. The value of this difference will be zero (neglecting the effects of noise on the data stream) when: (1) no data transitions have occurred during the early and late integrals, or (2) a data transition occurred at the time of the local estimate of the spacecraft data clock (bit time command). Thus, a phase-error value is not generated when transitions do not appear in the data or the local clock estimate is synchronous with the spacecraft clock. When the difference of the two squares is not zero, there is a phase error in the local estimate of the data clock. The sign of the difference corresponds to the minimum direction to shift the phase of the local estimate of the data clock to correct the phase error. The magnitude of the difference is proportional to the amount of phase shift necessary to correct the phase error.

The phase error signal is scaled to an equivalent number of microseconds of required phase shift. This positive, negative, or zero value is added to the basic data bit interval time in microseconds. The data bit duration (data rate frequency) is *a priori* information supplied to the computer program by the equipment operator at the beginning of the tracking pass. The combined value is then output by the computer to the digital phase shifter.

The digital phase shifter (DPS) performs the function of an oscillator that is programmable in frequency and phase. The DPS accepts an output from the computer consisting of the spacecraft data bit time duration combined with the amount of phase correction in microseconds necessary to bring the local data clock (bit timing command) estimate in coherence with the spacecraft data clock. This value is counted down at a 1-MHz rate by the DPS. When zero count is detected, the DPS is ready to accept new frequency and phase information from the computer. During the countdown, four pulses are output by the DPS to the timing generator. These four pulses are spaced in one-quarter increments of the duration of the countdown. The DPS, by periodically counting down numbers that are either larger or smaller than the expected duration of a telemetry bit interval, can effect a phase shift with a resolution of 1 μs on the series of the four output pulses. When a phase shift is not necessary, the DPS simply counts down data bit duration in microseconds.

The timing generator, by utilizing steering circuitry, provides the early, late, and bit timing commands to the A/DC and the computer. These commands control the sampling times of the three integrate and dump inputs to the computer.

Thus, one bit synchronization loop is able to adjust the phase, early, and late timing commands to the point where the difference of the squares of the early and late integrals

is zero (or at least to below correction threshold) to correct the phase of the local estimate of the data clock. When this occurs, the bit timing command is coherent with the spacecraft data clock, and it is a valid signal for use by the bit detection circuit. The computation of the loop phase error and the countdown by the DPS is repeated once during each bit time to either correct the phase of the bit timing command or to maintain the existing phase.

An equipment description of the computer and digital hardware is contained in Sect. E-2.

Telemetry data-frame synchronization, formatting. All formatting and decommutation on the detected telemetry data is accomplished by the computer software. This area contains the only mission-dependent portion of the MMTS. However, since these functions are totally performed by software, no equipment modifications are required to change from one flight project to another flight project. All that will be required is that each flight project furnish its own operational software to run in the MMTS computer.

Frame synchronization will be performed by examining the data table for the proper sequence of data bits to form the sync word as transmitted by the spacecraft. Thus, the data may be arranged in a table in an orderly sequence starting with each frame with a sync word.

Decommutation of the telemetry data is performed on the spacecraft engineering data as time allows in the computer. MMTS decommutation will extract selected measurements from the spacecraft engineering telemetry and route this information to the station monitor teletype output.

The telemetry data must be formatted for output from the computer. Formatting consists of coding or arranging the data for the various output devices, adding identification messages, and interspersing various MMTS performance indicators between data frames.

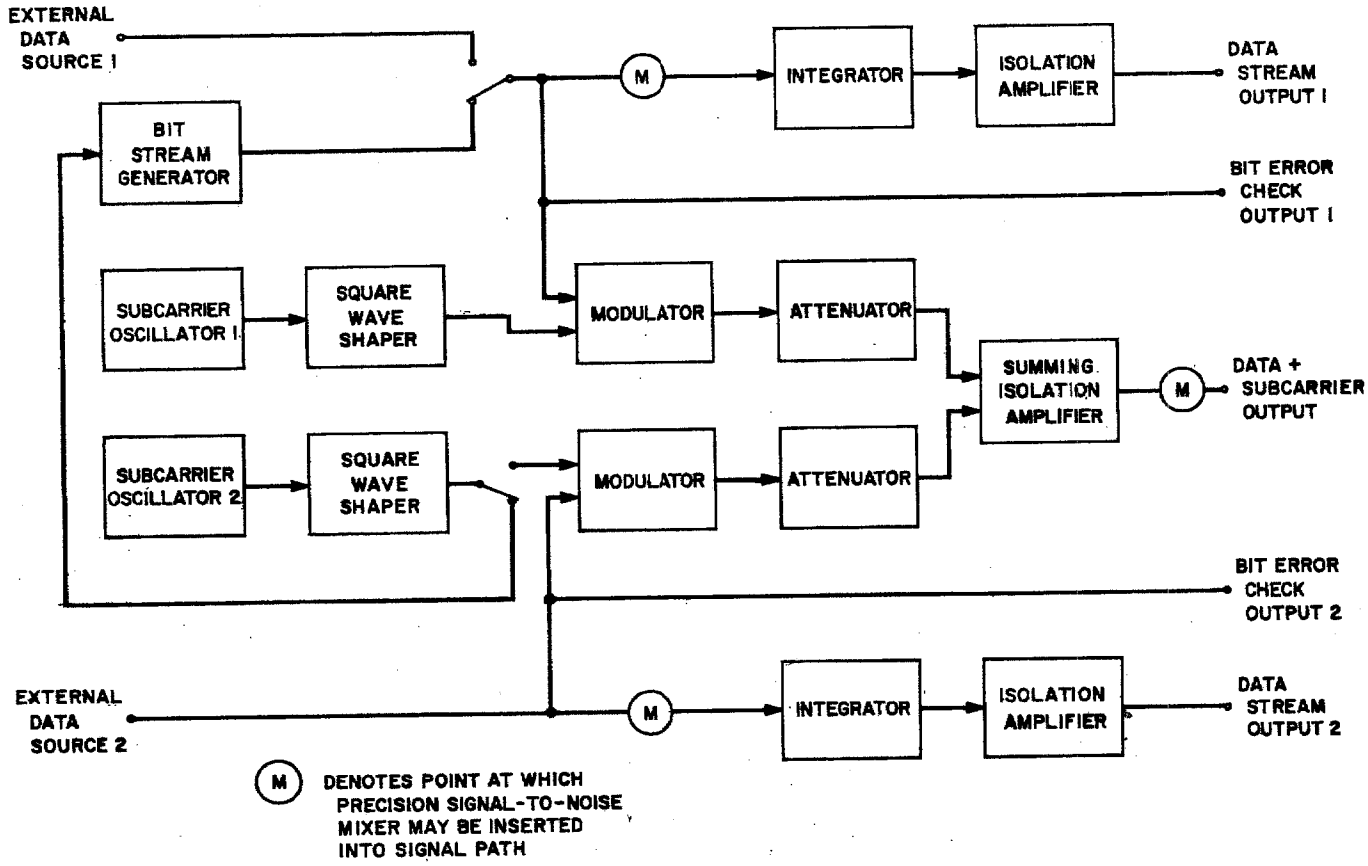


Fig. 2. MMTS test equipment block diagram

c. Test equipment. The objective of the MMTS test equipment is to provide a mission-independent set of equipment to evaluate the performance of the multiple mission telemetry equipment. A functional block diagram of the test equipment is shown in Fig. 2. The test equipment is housed in a rack that is provided to each of the DSIF stations where the MMTS has been implemented. The test equipment has been designed to allow for maximum flexibility in the testing of the MMTS equipment. Test signals provided by the equipment may be inserted into various areas of the receiver and MMTS equipment to evaluate system performance (Fig. 3). The test modes available and types of test signals provided are described in detail in the hardware description (Section E-4) of the test equipment.

Testing of the MMTS equipment consists of performing bit error tests on the telemetry data detected by the MMTS computer. Telemetry data is provided by a pseudo-random code generator located in the test equipment. This data either is integrated or modulates a test subcarrier to provide test inputs to the computer, the subcarrier demodulator assembly, or the DSIF test transmitter. The test signal is processed by the receiver and/or the MMTS as it would be in an operational configuration supporting a flight project. The test telemetry is recovered in the bit detector in the MMTS computer. The generated test telemetry data is also routed from the test equipment directly to the computer. Each bit that is output by the code generator is then compared with the recovered detected data by a software test subroutine in the computer. The subroutine keeps track of the number of disagreements of the compared data. These errors are counted for a prescribed number of bit inputs. This tally, which is equivalent to bit error rate (BER), is printed out on the computer console typewriter at the conclusion of each test. Tests are performed for various signal-to-noise conditions and subcarrier and data rate frequencies. The bit error-rate data generated by the computer is compared to charts that contain a theoretical performance curve of the equipment to detect performance degradation. These curves plot expected bit error rate versus various signal-

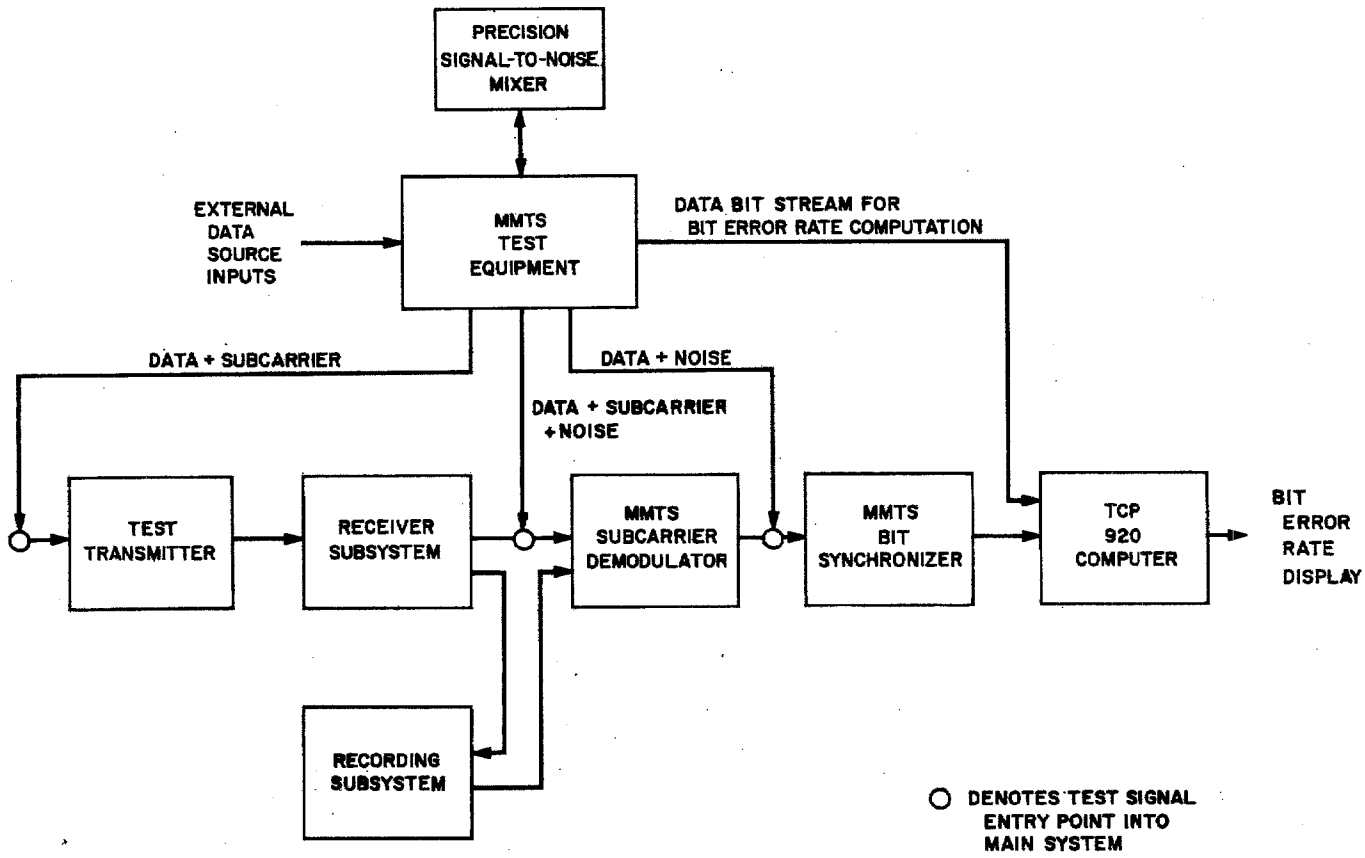


Fig. 3. Functional arrangement of test signals and equipment assemblies

to-noise conditions. The design goal of the MMTS is to allow a maximum of 0.2 of a dB performance degradation from the expected theoretical performance of the equipment over the range of signal-to-noise conditions which the MMTS will encounter in supporting the flight projects.

2. System Backup

The MMTS will have various back-up modes of operation in the event of equipment malfunction. The back-ups are provided to minimize the amount of telemetry data lost in the event of an MMTS equipment failure. Each DSIF station will be supplied with redundant channels of the subcarrier demodulator assembly and the computer and digital equipment assembly. When a flight project is operating with two subcarrier frequencies simultaneously, each channel of the MMTS will be committed to process a subcarrier and data rate. However, during periods when a single subcarrier is being transmitted from the spacecraft, the second MMTS channel serves as a back-up. When both channels are committed, or failure in both channels occurs, the following additional back-ups are available.

a. Subcarrier demodulator back-up recording. In the operational configuration of the MMTS in the net, an analog magnetic tape recording is made of the baseband output (subcarrier modulated with data) from the telemetry channel of the receiver. In the case where a failure occurs in either or both SDAs, the following back-up procedure is taken. The baseband recording is kept intact until such time as the repairs can be made to the SDA. The tape is then played back through the baseband input of the SDA. The baseband input (Fig. 1, point 9) modulates a 10-MHz reference in the up-converter. The output of the up-converter is a replica of the normal 10-MHz IF telemetry output provided by the receiver. Therefore, the tape can be played back through the entire MMTS in non-real-time to recover any of the telemetry data lost in real-time due to failures in the SDAs. A degradation of the performance of the MMTS is encountered in this mode, due to limitations in the bandwidth capability and time base instability of the tape recorder.

b. Computer and digital equipment back-up recording. In the normal operation of the MMTS, a magnetic recording is made of the data stream output of the subcarrier demodulator assembly. Should a failure occur in the computer and digital equipment, this recording is played back in non-real-time into the data stream input of the computer equipment to recover the telemetry data. No appreciable degradation in performance is encountered in this playback mode.

c. Ground communications system back-up recording. Should a failure occur in the GCS (high-speed data line or teletype lines) which results in loss of the transmitted data, use is made of the digital magnetic tape recording of the formatted telemetry data. This recording is made in real-time at the TCP-IIC equipment. The recording may be played back through the computer and output to the GCS, when communications are restored, or it may be mailed from the station to the SFOF for off-line processing at a later date.

3. MMTS Software

A computer program must be provided to the MMTS computer in order to accomplish bit synchronization, bit detection, formatting, and the output of the telemetry data. Two categories of software will be provided to the system. The first program type is the demonstration software. The demonstration software is being written by and for the MMTS project. This program will be used in the MMTS demonstration system. The demonstration system (described in Sect. D) consists of prototype hardware which will remain at JPL and will be used to test and evaluate MMTS performance and design parameters. The demonstration program will be provided to evaluate the mission-independent software functions and assist in performing hardware tests in the demonstration system. A description of the demonstration program appears in Sect. E-3.

The second type of MMTS software is the operational software. The operational software will be supplied to the MMTS computers at the DSIF stations and will be written under the direction of the flight projects. The operational software performs both mission-independent and mission-dependent functions. The *Mariner* Mars 1969 flight project program will be described in a future SPS article. The MMTS project will issue specifications on hardware restrictions and timing constraints placed on the software by the MMTS equipment to assist the flight projects in preparing the operational software.

4. MMTS Implementation into the DSIF

MMTS equipment will be implemented into the DSIF in all stations. Each station will receive two MMTS channels. Initially, the stations that will be supporting the *Mariner* Mars 1969 flight projects will be implemented. The remaining stations will be implemented at a later

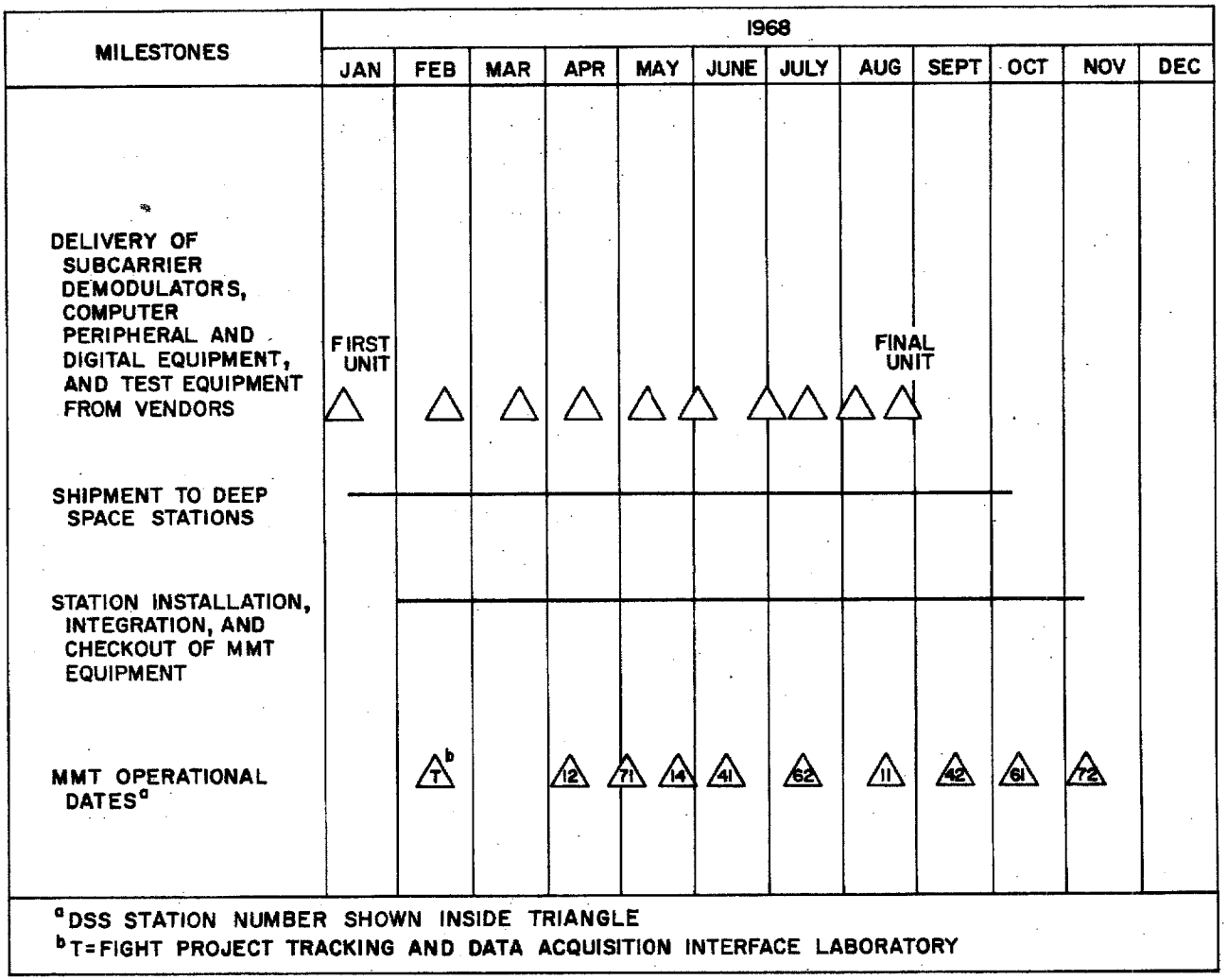


Fig. 4. MMTS implementation schedule

time. Figure 4 contains an implementation schedule showing dates for shipment, installation, checkout, and operational readiness for the MMTS equipment at each of the DSIF stations. In addition to the net systems, the project will supply a single-channel MMTS to the flight project/tracking and data acquisition interface laboratory located at JPL. The delivery of this equipment is also included in the schedule.

5. Operation of MMTS in the DSIF

a. A priori knowledge required for operation. The operation of the MMTS in the net requires *a priori* knowledge to be provided to the operators of the equipment. This required information is obtained from either the Tracking Instruction Manual which is provided to the station for each project, or from the daily prediction information transmitted by teletype to the station from the SFOF. The operators of the SDA and the computer and digital equipment require the following information for operating the MMTS equipment:

(1) Spacecraft subcarrier frequency.

(2) Spacecraft telemetry data rate.

(3) Nominal signal-to-noise ratio.

(4) Subcarrier modulation index.

(5) Doppler frequency rate.

b. MMTS operational procedures. The following description pertains to the procedures used by the operators of the MMTS equipment to obtain an output from the

computer of the detected and formatted telemetry data. The acquisition of the telemetry data by the MMTS is a two-step process. First, the SDA must be locked to the incoming subcarrier and secondly, the computer and digital equipment must lock up the bit synchronization loop. Operational procedures to accomplish these two steps will be described and are based on the assumption that the operators have received the required *a priori* information listed in Sect. B-5-a.

Lock of the SDA. The following steps are taken by the operator to lock the SDA to the incoming subcarrier frequency:

(1) Verify that the RF carrier loop is in lock.

(2) Set the SDA input attenuator based on the submodulation index information.

(3) Select the spacecraft subcarrier frequency at the synthesizer.

(4) Preset the predetection filter, postdetection filter, and the data integrator time-constant selector switch.

(5) Set the loop bandwidth selector switch based on the signal-to-noise condition, doppler rate, and telemetry data rate.

(6) Short the output of the loop filter.

(7) Adjust acquisition control voltage for zero beat frequency of the dynamic phase error.

(8) Remove the short from the output of the loop filter.

The loop will then pull into lock.

Bit synchronization loop lock acquisition. The following procedures are taken by the operator at the computer and digital equipment to obtain bit synchronization lock:

(1) Verify that proper patch panel configuration is being used to input data signals from the SDA.

(2) Load the computer with MMTS operational program.

(3) Input to the computer values of nominal signal-to-noise ratio and telemetry bit rate. Input is either by paper tape or via computer typewriter.

Once the operator has provided inputs of signal-to-noise ratio and data rate, the remaining portion of the bit synchronization process is automatic and under control of the software. The operator is informed by the program when acquisition is complete via a message typed out on the computer typewriter.

c. MMTS performance monitoring. After the acquisition phase is complete and the subcarrier and bit synchronization loops are in lock, information is provided by the MMTS to the station monitoring computer to evaluate performance and verify proper configuration. The following indicators are provided:

(1) Subcarrier demodulator assembly input switch setting.

(2) SDA predetection filter, postdetection filter, and data integrator switch setting.

(3) SDA loop bandwidth switch setting.

(4) SDA output switch setting.

(5) SDA loop static phase error (SPE)—analog signal.

(6) SDA loop dynamic phase error (DPE)—analog signal.

(7) SDA acquisition voltage value—analog signal.

(8) SDA VCO–synthesizer frequency. (This output must be counted external to the SDA in order to be monitored.)

(9) SDA data rate option (medium or low).

(10) SDA in–out lock status.

(11) Signal-to-noise ratio of the telemetry data stream.

(An estimate of the signal-to-noise ratio of the telemetry data stream is calculated by the MMTS computer. This information is transmitted by the MMTS computer to station monitor equipment. The station monitor computer compares the calculated signal-to-noise ratio to the expected nominal signal-to-noise ratio. If these two numbers agree by a specified tolerance, the performance of the MMTS is considered good. Should the number disagree by more than the specified tolerance, the station monitor will provide an alarm indication of unacceptable performance of the MMTS.)

6. MMTS Testing

The MMTS project is currently in the design and development phase. During this period, it is necessary to verify that the hardware performance meets the design and analysis criteria. To conform to this requirement, a laboratory prototype MMTS will be provided. This equipment will be known as the "demonstration system."

Demonstration software will also be supplied by the project to assist in the evaluation of the hardware performance. A description of the demonstration system verification testing is contained in Section D of this article. Knowledge gained by the demonstration system testing will result in improvements and refinements in the MMTS equipment design before it is implemented to the DSIF.

The first operational MMTS which conforms to the final design will be provided to the new JPL Flight Project/Tracking and Data Acquisition Interface Laboratory. The function of this facility will be to demonstrate telecommunications compatibility of the spacecraft, DSIF ground equipment, ground communications system, and the SFOF. The MMTS will undergo compatibility testing with the existing DSIF ground equipment and the total telecommunications link. This facility will also provide a simulation of the DSIF environment for checkout of the flight project operational software.

The MMTS equipment implemented into the DSIF will be subjected to extensive testing when it is installed and becomes operational. Testing will continue throughout the useful life of the equipment.

a. Installation integration testing. The testing of the MMTS at the time of installation in the DSIF stations will verify proper interfaces with other subsystems in the station and establish that the MMTS is operating to the required design goals. The criteria and procedures for this testing will be originated by the MMTS project.

b. Postinstallation testing. Once installed and operational, the MMTS will undergo the following types of tests:

DSN compatibility testing. For each flight project that the MMTS supports, requirements will exist for compatibility testing. The purpose of this testing is to demonstrate hardware and operational software compatibility of the DSIF, the ground communications system, and the SFOF. Verification of proper MMTS performance and operator training, under simulated mission conditions, will be obtained in these tests. The compatibility tests are performed prior to the launch of a spacecraft and are generated by the DSN project engineer for the flight project.

Performance evaluation testing. This test is performed periodically on the MMTS to verify that the equipment is operating properly and has not suffered any degradation of performance. These tests will be defined by the MMTS project.

Configuration verification testing. This test is performed on the DSIF station prior to each spacecraft launch to verify that the station (including the MMTS) is in the proper configuration to support the flight project. These tests are originated by the operations engineering group in the DSIF.

Countdown tests. Tests will be performed on the MMTS during the station countdown prior to tracking pass. These tests will provide a daily evaluation of the performance of the MMTS. These tests are defined by the DSIF station managers.

C. System Performance and Analysis,

M. H. Brockman, R. W. Burt, J. W. Layland, and G. M. Munson

1. Introduction, *G. M. Munson and R. W. Burt*

This section is divided into three parts. First is a general discussion of the telemetry system bit-error rate performance which is contained in Sect. 2. The other two parts are detailed examinations of the performance of the subcarrier demodulator and the bit-synchronization loop.

An analysis of the subcarrier demodulator is presented in Sect. 3. The first portion of this analysis is a development of a linear model. Design curves are presented relating loop phase error to ST_B/N_0 for various loop bandwidths. Then the parameters associated with low- and medium-rate telemetry are applied to the model.

Section 4 contains an analysis of the bit-synchronization loop. Models for first- and second-order loops are examined, and the expected value and variance of the bit-timing error are derived. The effect of the bit-timing jitter is determined in terms of degradation of ST_B/N_0. Initial acquisition requires a special procedure. A discussion of this procedure is included. The effects of nonlinearities of the loop are also examined.

2. MMTS Bit Error-Rate Performance

The performance of a digital telemetry receiver is judged by the bit-error rate of the output bit stream, given a received signal power. The output bit-error rate of the MMTS depends on four fundamental parameters in addition to the input sideband signal-to-noise energy ratio in a bit period. These parameters become evident when the simplified block diagram of the system as shown in Fig. 5 is examined.

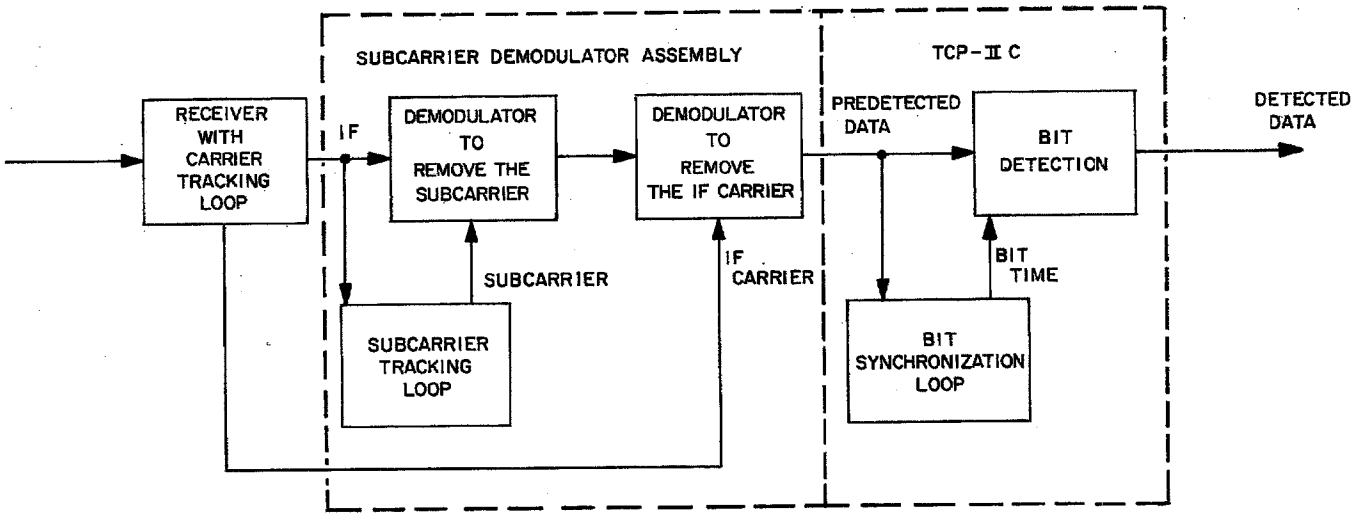


Fig. 5. Simplified block diagram of SDA and TCP-II C

a. The general equation. The general equation for effective sideband signal-to-noise energy ratio is given in Eq. (1).

$$R = \frac{ST_B}{N_0}(\alpha)(\beta)(\gamma)(\delta) \qquad (1)$$

where

R = effective sideband signal-to-noise energy ratio per bit.

$\frac{ST_B}{N_0}$ = input sideband signal-to-noise energy ratio per bit.

α = degradation caused by the IF reference error.

β = degradation caused by the subcarrier reference error.

γ = degradation caused by the bit synchronization error.

δ = degradation caused by the bit detection process.

The flight project controls the α parameter by the design of the radio link and the modulation index. A design goal has been established for each of the other three parameters. This goal is 0.1 dB maximum degradation when the probability of bit error for the output bit stream is 0.1. The system will degrade slowly as ST_B/N_0 decreases. The point at which improving signal-to-noise energy ratio does not improve the bit error rate has not been determined at this time.

b. IF reference error α. The phase error between the IF carrier signal and the IF carrier reference results in a degradation of the effective ST_B/N_0. The degree of degradation may be determined with methods developed by Lindsey in SPS 37-45, Vol. IV, pp. 276–282, using the received signal level, modulation index, and receiver characteristics. The receiver's carrier loop bandwidth is much larger than subcarrier loop bandwidth. This minimizes interaction between the loops and permits usage of Lindsey's analysis.

c. Subcarrier reference error β. The reduction of effective ST_B/N_0 due to the subcarrier phase is caused by two types of phase error. A static error occurs due to doppler and doppler rate tracking. A dynamic phase error occurs due to receiver and oscillator noise. At low values of ST_B/N_0, the dynamic phase error is the more significant of the two. An analysis of the subcarrier demodulator performance is presented in Sect. C-3. An expansion of this analysis (to be published in a future SPS) will show that

$$\beta = 1 - \left(\frac{2}{\pi}\right)^{3/2} \sigma_{\phi n_{sc}}$$

where $\sigma_{\phi n_{sc}}$ = rms phase noise error in the subcarrier tracking loop and $3\,\sigma_{\phi n_{sc}} < \pi/2$ rad.

d. Bit synchronization error γ. The bit synchronization error term γ modifies the input sideband signal-to-noise energy ratio by accounting for errors in estimated transition time. This term is dependent upon the received bit stream. If a transition does not occur, no degradation

results. If a transition does occur, the probability of correct detection is reduced.

For a bit stream which has a probability of transition of approximately 0.5, the degradation of ST_B/N_0 is

$$\gamma = \tfrac{1}{2} + \tfrac{1}{2}\int_{-\frac{1}{2}}^{\frac{1}{2}} p(\tau)\,[1 - 2|\tau|]^2\,d\tau$$

where τ is the error between estimated and actual transition time, and $p(\tau)$ is the probability density function of τ, the timing error.

The problems of bit synchronization and the effects of bit error rate are discussed in part 4 of this section.

e. Bit-detection error δ. At this time, the degradation caused by the bit-detection process δ has not been completely analyzed. Initial examinations indicate this degradation will be small with respect to the other parameters.

3. MMTS Subcarrier Demodulator, *M. H. Brockman*

a. General analysis

Functional description. Figure 6 is a functional block diagram for the MMTS subcarrier demodulator. The input signal is an RF signal at the IF frequency of the DSIF receiver. The DSIF receiver phase tracks the received carrier and heterodynes it to the IF frequency at a fixed phase. The received signal contains telemetry data in the form of a binary waveform which biphase modulates a square-wave subcarrier. The modulated subcarrier, which is also a binary waveform, in turn phase modulates the carrier. The purpose of the MMTS subcarrier demodulator is to recover the original binary telemetry waveform by synchronously demodulating both the carrier and the subcarrier. The DSIF receiver provides a reference signal at 10 MHz to demodulate the carrier. The reference signal to demodulate the subcarrier is provided by the MMTS demodulator itself, a portion of which acts as a phase-locked loop to track the subcarrier. Both demodulation processes take place in the upper channel of Fig. 6.

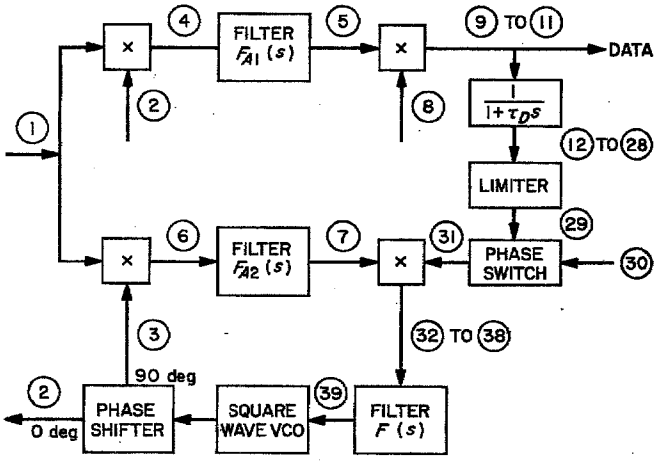


Fig. 6. Telemetry subcarrier demodulator functional block diagram

For circuitry reasons associated with the need to accommodate a wide range of subcarrier frequencies, the subcarrier demodulation is performed first. The output of the upper channel is the recovered binary waveform which is sent to another part of the overall system for detection. The output waveform is also filtered and limited to provide an estimate of the binary waveform (the recovered waveform is typically contaminated with noise and not strictly binary) that is used in the lower channel. The lower channel operating with the filter and VCO forms the basic subcarrier tracking loop. However, since the original telemetry waveform biphase modulates the subcarrier and thus inverts it whenever the telemetry waveform is negative, the subcarrier tracking loop is trying to track a wave which is inverted part of the time (ideally 50% of the time). The estimate of the telemetry waveform produced by filtering and limiting the output of the upper channel is injected into the tracking loop by modulating the reference of the 10-MHz synchronous demodulator. This has the effect of reinverting the subcarrier, although it actually acts on the error signal in the loop.

Predemodulation signal and noise. In the following simplified analysis, refer to the block diagram shown in Fig. 6.

Assumption. *The performance of the various elements of the demodulator are considered ideal, and circuit performance imperfections are not considered. The effect of such imperfections will be considered in a later report. It is also assumed that the RF carrier received from the spacecraft is a spectral line or, alternately, that the phase instability of the spacecraft RF carrier is such that the DSIF RF carrier phase-locked loop can track this phase instability with negligible phase error. In addition, the waveform of the received telemetry subcarrier is assumed to be a perfect square wave.*

The input signal is an RF signal (at IF frequency f_2 Hz or ω_2 rad/s) phase modulated with a square wave telemetry subcarrier (ω_{sc}) which is, in turn, biphase-modulated with the data $m(t)$.

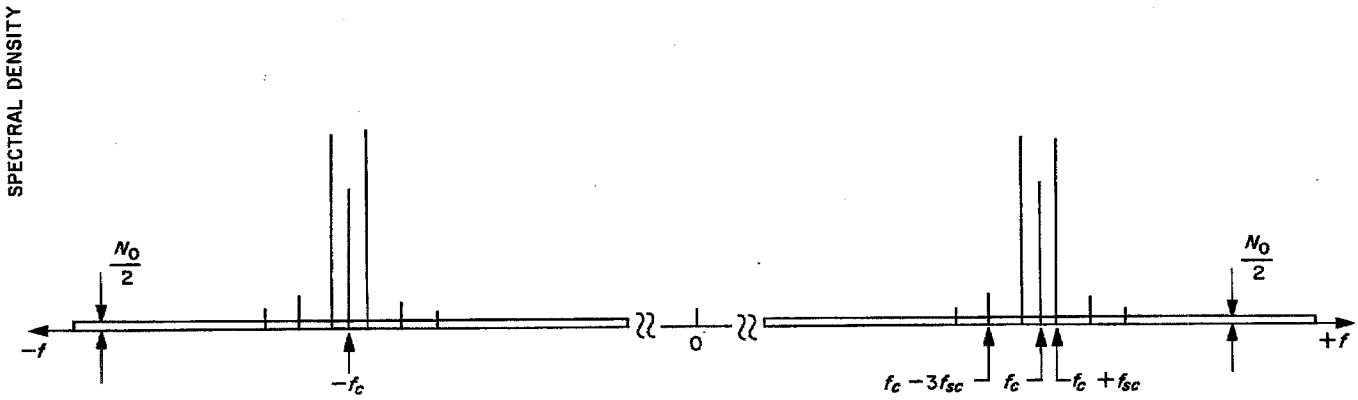


Fig. 7. Spectral power density for input signal to subcarrier demodulator

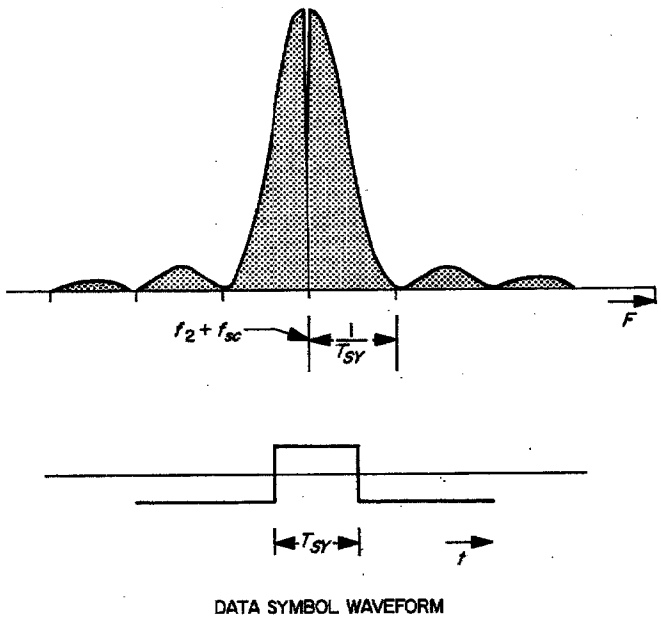


Fig. 8. Data power spectrum about subcarrier fundamental

$$(2)^{1/2} A \cos\left[\omega_2 t + (m(t) \times m_{ps} \times \cos(\omega_{sc} t + \theta)\right] + n_2(t) \tag{1a}$$

where m_{ps} is the peak phase-modulation index in radians (due to telemetry), and $m(t)$ is plus or minus 1, depending on the data. The term θ is the input telemetry subcarrier phase, which is considered as nontime varying in this simplified analysis. The term $n_2(t)$ represents input receiver noise (Gaussian and white) for the receiver bandwidth at this point in the system which has a double-sided noise spectral density of $N_0/2$. $N_0/2 = \frac{1}{2}(k \times T \times 1)$ W/Hz, where k is Boltzmann's constant, 1.38×10^{-23} J/°K, and T is the equivalent noise temperature of the receiving system. Total input signal power is A^2, where $A << 1$ (an impedance of unity is assumed to simplify the expression for power).

Figure 7 shows a spectral power density representation for the input signal and noise for both positive and negative frequencies. A specific modulation index, m_{ps}, is also depicted. In general, the relative magnitude of the RF carrier and subcarrier spectral lines will change with change in modulation index. The subcarrier spectra about the RF signal at f_2 are shown as spectral lines on the scale of Fig. 7. In reality, the subcarrier fundamental spectral line and all its harmonic spectral lines consist of the power spectrum of the data $m(t)$ about them as illustrated in Fig. 8 (for $f_2 + f_{sc}$). The data power spectrum is shown as continuous, which assumes that the data changes somewhat from one data frame to the next. The envelope of the data power spectrum is determined by the square wave shape of the data symbol waveform.

Because the modulation waveform is binary, Expression (1a) can be written as

$$\underbrace{(2)^{1/2} A \cos m_{ps} \cos \omega_2 t}_{\text{carrier}} + \underbrace{(2)^{1/2} A \sin m_{ps} \times m(t) \times \cos(\omega_{sc} t + \theta) \times \sin \omega_2 t + n_2(t)}_{\text{sidebands}} \tag{1b}$$

The signals obtained from the square wave subcarrier VCO at ② and ③ may be written as

$$\cos(\omega_{sc} t + \hat{\theta}(t)) \tag{2}$$

and

$$\sin(\omega_{sc} t + \hat{\theta}(t)) \tag{3}$$

where $\hat{\theta}(t)$ is the loop estimate of θ, the subcarrier input phase. The input signal, Expression (1b), is multiplied by the square wave cosine subcarrier signal, Expression (2), to provide Expression (4):

$$(2)^{1/2} A \cos m_{ps} \cos [\omega_{sc} t + \hat{\theta}(t)] \cos \omega_2 t + (2)^{1/2} A \sin m_{ps} \times m(t) \times \cos [\omega_{sc} t + \theta] \cos [\omega_{sc} t + \hat{\theta}(t)] \sin \omega_2 t + n_4(t) \quad (4)$$

where the noise term $n_4(t)$ is $n_2(t)$ in Expression (1b) multiplied by $\cos [\omega_{sc} t + \theta(t)]$.

Assumption. The assumption has been made here that the relative broadening of the noise spectrum (shown in Fig. 7) due to this multiplication is small enough to be ignored. Therefore, the noise term, $n_4(t)$, at ④ in Fig. 6 has a double-sided noise spectral density of $N_0/2$ and the same total noise power as $n_2(t)$. This is a conservative assumption.

After passing through the upper predemodulation filter F_{A1}, Expression (4) becomes

$$F_{A1} \{(2)^{1/2} A \cos m_{ps} \times \cos [\omega_{sc} t + \hat{\theta}(t)] \times \cos \omega_2 t + (2)^{1/2} A \sin m_{ps} \times m(t) \times \cos [\omega_{sc} t + \theta] \times \cos [\omega_{sc} t + \hat{\theta}(t)] \sin \omega_2 t\} + n_5(t). \quad (5)$$

The noise term $n_5(t)$ represents the receiver noise at the upper predemodulation filter output with a double-sided noise spectral density (positive and negative frequencies) of $N_0/2$. The ratio of noise powers represented by $n_5(t)$ and $n_2(t)$ is equal to the ratio of the noise bandwidths at ⑤ and ① in Fig. 6. The noise term $n_5(t)$ is centered about f_2. The first term of Expression (5) would normally be removed by the predemodulation filter F_{A1}, although this is not a requirement.

The input signal, Expression (1b), is multiplied in the lower multiplier in Fig. 6 by the square wave sine subcarrier signal, Expression (3), to provide Expression (6):

$$(2)^{1/2} A \cos m_{ps} \sin [(\omega_{sc} t + \hat{\theta}(t)] \times \cos \omega_2 t + (2)^{1/2} A \sin m_{ps} \times m(t) \times \cos [\omega_{sc} t + \theta] \sin [\omega_{sc} t + \hat{\theta}(t)] \times \sin \omega_2 t + n_6(t) \quad (6)$$

where the noise term $n_6(t)$ is $n_2(t)$ in Expression (1b), multiplied by $\sin [\omega_{sc} + \theta(t)]$.

Assumption. Again the assumption has been made that the relative broadening in the noise spectrum of Fig. 7 due to this multiplication is small enough to be ignored. Therefore, the noise term, $n_6(t)$, at ⑥ in Fig. 6 has a double-sided noise spectral density of $N_0/2$. This is, again, a conservative assumption.

After passing through the lower predemodulation filter F_{A2}, Expression (6) becomes:

$$F_{A2} \{(2)^{1/2} A \cos m_{ps} \sin [\omega_{sc} t + \hat{\theta}(t)] \times \cos \omega_2 t + (2)^{1/2} A \sin m_{ps} \times m(t) \times \cos [\omega_{sc} t + \theta] \sin [\omega_{sc} t + \hat{\theta}(t)] \times \sin \omega_2 t\} + n_7(t) \quad (7)$$

The noise term $n_7(t)$ represents the receiver noise at the lower predemodulation filter output with double-sided noise spectral density of $N_0/2$. Ideally, F_{A2} is equal to F_{A1}. Again, the ratio of noise powers presented by $n_7(t)$ and $n_2(t)$ is equal to the ratio of noise bandwidths at ⑦ and ① in Fig. 6. The noise term $n_7(t)$ is centered about f_2. Further investigation of Expression (7) will be made later in this report.

Coherent demodulation of data waveform

The reference signal at ⑧ in Fig. 6 is

$$(2)^{1/2} \sin \omega_2 t \quad (8)$$

Assumption. It is assumed for the present that the received carrier power is such that the phase noise error in the RF carrier tracking loop is small enough so that it can be ignored.

The output of the upper linear coherent demodulator is the multiplication of Expression (5) by Expression (8) which provides (ignoring double frequency terms which are filtered out and orthogonal terms):

$$m(t) A \sin m_{ps} \{\cos [\omega_{sc} t + \theta] \cos [\omega_{sc} t + \hat{\theta}(t)]\} + n_9(t) \quad (9)$$

Assumption. Assume, for the present, that $\theta - \hat{\theta}(t)$ is small compared to $\pi/2$ rad. Consequently, the product of the two square wave cosine terms is unity.

Since $m(t) = \pm 1$, the signal power in Expression (9) is

$$P_s = A^2 \sin^2 m_{ps} \quad (10)$$

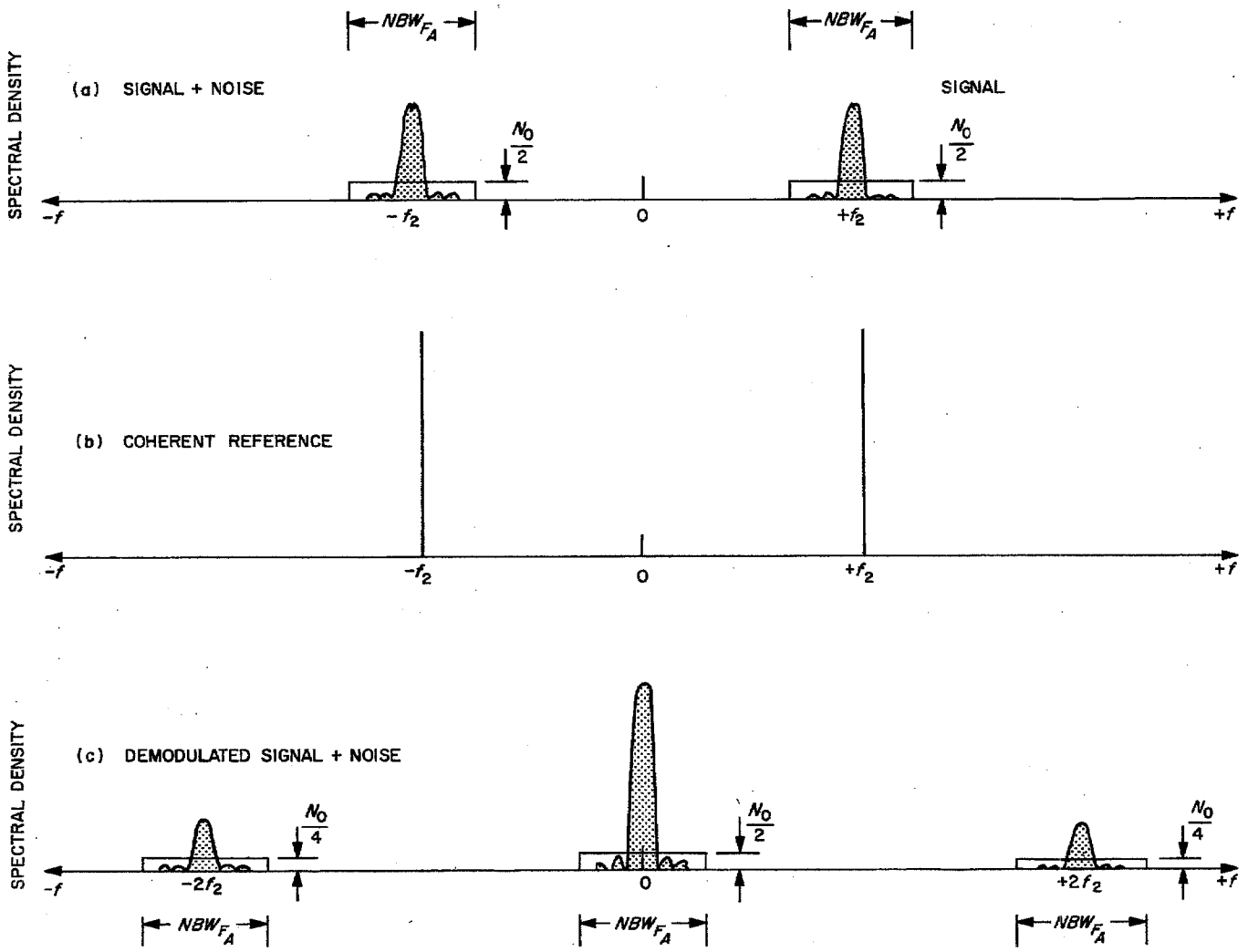


Fig. 9. Coherent data waveform demodulation

Consider next the noise term $n_0(t)$ in Expression (9). Figure 9 is a power spectral density representation of the coherent demodulation process. Figure 9(a) represents the signal plus noise into the coherent detector (second and third terms of Expression 5). The coherent reference signal (Expression 8) is represented by Fig. 9(b). Multiplication of signal plus noise by the coherent reference signal is shown in Figure 9(c). The multiplication process for each of the positive and negative frequency intervals about f_2 reduces the noise spectral density about $\pm 2f_2$ and about zero to $N_0/4$. The noise contributions from each of the positive and negative frequencies centered about zero frequency overlap to provide a resultant noise spectral density of $N_0/2$. Consequently, the power represented by the noise term in Expression (9) is equal to $N_0/2$ times the predetection filter noise bandwidth ($NBW_{F_{A1}}$). Hence, for the condition that the upper linear coherent demodulator has an output bandwidth (a low-pass zonal filter) which does not affect the spectral density representation (shown in Fig. 8) about zero frequency, the data signal-to-noise power ratio at ⑨ in Fig. 6 is

$$\frac{P_S}{P_N} = \frac{A^2 \sin^2 m_{ps}}{\frac{N_0}{2} \times NBW_{F_{A1}}} \tag{11}$$

Data waveform filtering. The data waveform filter has a time constant τ_D. Noise power at the output of the filter is

$$P_N = \int_{-\infty}^{+\infty} \Phi_N \frac{1}{1 + \tau_D^2 \omega^2} d\omega \tag{12}$$

which can be expressed as

$$P_{N_\tau} = \frac{N_0}{2}\frac{1}{2\pi}\int_{-\infty}^{+\infty}\frac{1}{\tau_D^2}\frac{1}{\frac{1}{\tau_D^2}+\omega^2}\,d\omega \tag{13}$$

where $\Phi_N = N_0/2 \times 1/2\pi$ is the noise spectral density in units of noise power per radian per second. Evaluation of this integral provides

$$P_{N_\tau} = \left(\frac{N_0}{2}\times\frac{1}{2\pi}\right)\times\frac{\pi}{\tau_D} = \frac{N_0}{2}\times\frac{1}{2\tau_D} \tag{14}$$

Since the noise is Gaussian, the noise power is

$$P_N = \sigma_N^2 \text{ (the variance)} \tag{15}$$

Consequently, the rms noise voltage is

$$\sigma_{nv_\tau} = \left(\frac{N_0}{2}\times\frac{1}{2\tau_D}\right)^{1/2} \text{ rms amplitude} \tag{16}$$

The amplitude of the demodulated data signal (from Expression 9) is $m(t)\,A\sin m_{ps}$ where $m(t)$ is ± 1 as determined by the data. Figure 10 shows the detected data signal during a transition of $m(t)$ from -1 to $+1$ which, in turn, is applied to the time constant τ_D. The resultant output signal from the time constant τ_D following such a transition is

$$m(t)\,A\sin m_{ps}\,(1-2e^{-t/\tau_D}) \tag{17}$$

where $t = 0$ at the transition. This waveform is also shown in Fig. 10. Consequently, the signal-to-noise voltage ratio at the data waveform filter output at time t (following a transition) can be obtained from Expressions (16) and (17)

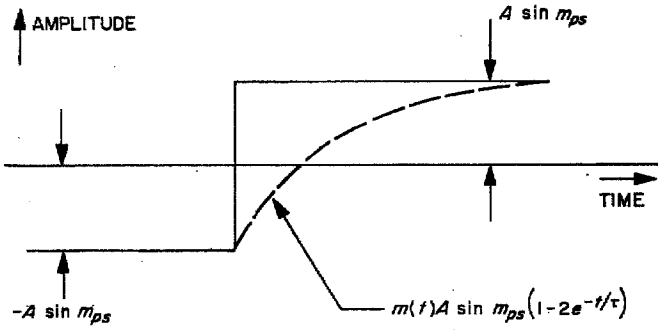


Fig. 10. Data waveform filter signal output waveform

$$(S/N)_v = \left|\frac{A\sin m_{ps}}{\sigma_{nv}}\times(1-2e^{-t/\tau_D})\right| \tag{18}$$

$$= \left|\frac{A\sin m_{ps}}{\left(\frac{N}{2}\times\frac{1}{2\tau_D}\right)^{1/2}}\times(1-2e^{-t/\tau_D})\right|$$

Designate the ratio $\tau_D/T_{SY} = \beta$, where T_{SY} is equal to the time duration of a data symbol. The signal-to-noise voltage ratio shown in Expression (18) can now be written as (substituting $\tau_D = \beta T_{SY}$)

$$(S/N)_v = \left|\frac{A\sin m_{ps}}{\left(\frac{N_0}{2}\times\frac{1}{2\beta T_{SY}}\right)^{1/2}}\times(1-2e^{-t/\beta T_{SY}})\right| \tag{19}$$

The variation in relative signal-to-noise voltage ratio (at the data waveform filter output) following a transition is shown in Fig. 11, plotted as a function of the ratio $\tau_D/T_{SY} = \beta$ at time equal to T_{SY} (that is, at the end of a data symbol). The signal-to-noise voltage is maximized when $\tau_D/T_{SY} = 1/2.48$. Relative signal-to-noise voltage ratio at $t = T_{SY}$ normalized to the maximum value for $\tau_D/T_{SY} = 1/2.48$ is

$$\text{Rel}\,(S/N)_v = \frac{\left|\frac{A\sin m_{ps}}{\left(\frac{N_0}{2}\times\frac{1}{2\beta T_{SY}}\right)^{1/2}}\times(1-2e^{-1/\beta})\right|}{\left|\frac{A\sin m_{ps}}{\left(\frac{N_0}{2}\times\frac{2.48}{2T_{SY}}\right)^{1/2}}\times(1-2e^{-2.48})\right|} \tag{20}$$

$$= \left|(2.48\,\beta)^{1/2}\times\frac{(1-2e^{-1/\beta})}{(1-2e^{-2.48})}\right|$$

$$= \left|\left(2.48\frac{\tau_D}{T_{SY}}\right)^{1/2}\times\frac{(1-2e^{-T_{SY}/\tau_D})}{(1-2e^{-2.48})}\right|$$

Maximum signal-to-noise voltage ratio is

$$\text{Max}\,(S/N)_v = \frac{A\sin m_{ps}}{\left(\frac{N_0}{2}\times\frac{1.24}{T_{SY}}\right)^{1/2}}\times(1-2e^{-2.48}) \tag{21}$$

$$= \frac{A\sin m_{ps}}{\left(\frac{N_0}{2}\times\frac{1.24}{T_{SY}}\right)^{1/2}}\times 0.8325$$

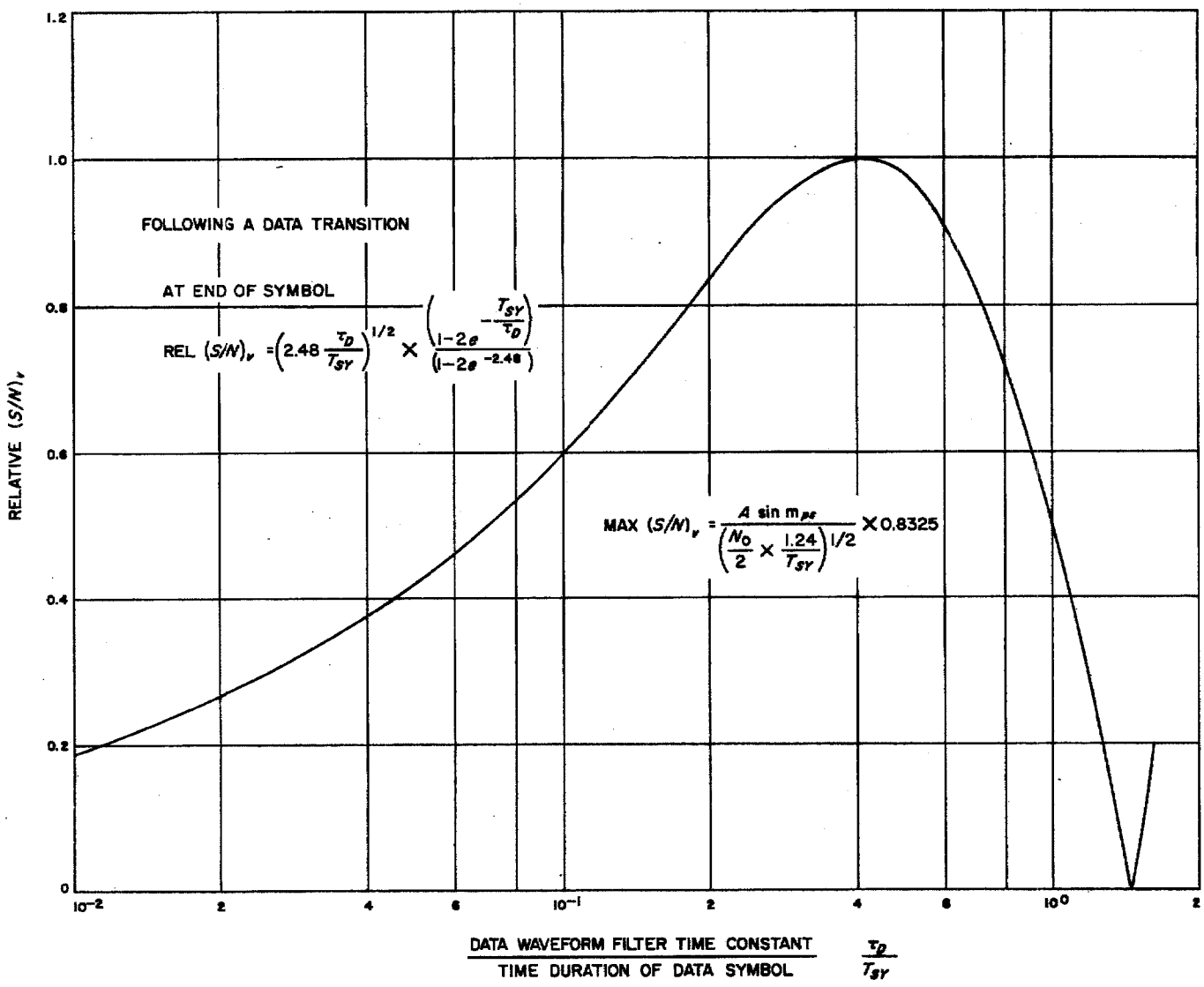


Fig. 11. Relative signal-to-noise voltage ratio versus ratio of data waveform filter time constant to data symbol time duration

Limiter characteristic and subcarrier loop error signal. The observed voltage at the output of the data waveform filter consists of filtered signal plus noise

$$v(t) = s^*(t) + n(t) \tag{22}$$

At a particular time

$$V = S_\tau^* + N_\tau \tag{23}$$

From Expression (17), the filtered signal is

$$s^*(t) = m(t) A \sin m_{ps} (1 - 2e^{-t/\tau_D}) \tag{24}$$

The undistorted or ideal signal is

$$s(t) = m(t) A \sin m_{ps} \tag{25}$$

which is a binary waveform that switches between two values ($\pm S_v$) corresponding to whether $m(t)$, the data, is $+1$ or -1 which, in turn, corresponds to a binary 0 or 1. Note that for $t >> \tau_D$ following a data transition, $s^*(t)$ and $s(t)$ become identical; consequently, $S_v^* = S_v$ $(t >> \tau_D)$.

Assume, for the present, that the transition (switching) of the binary data signal waveform from $+1$ to -1, or vice versa, is random with a 50% probability that it does

not switch from one symbol period to the next and, of course, 50% probability that it does switch[2] (for example, as determined by a sequence of flips of an unbiased coin). The signal at the input to the limiter (following the data waveform filter, Fig. 6), during any given symbol period, represents either of two situations: Either there has *not* been a transition from $+S_v$ to $-S_v$ (or vice versa) at the beginning of the period, or there has been a transition. Designate the first type of symbol period as $T_{SY_{11}}$ or $T_{SY_{00}}$ and the second type as $T_{SY_{01}}$ or $T_{SY_{10}}$. The observed voltage V given S_v (signal is present) has a probability density function

$$p(V/S_v) = \frac{1}{(2\pi)^{1/2}\,\sigma_{nv}} \exp\left[-\tfrac{1}{2}\left(\frac{V - S_v^*}{\sigma_{nv}}\right)^2\right] \qquad (26)$$

which is shown sketched in Fig. 12 for a $T_{SY_{00}}$ type symbol period.

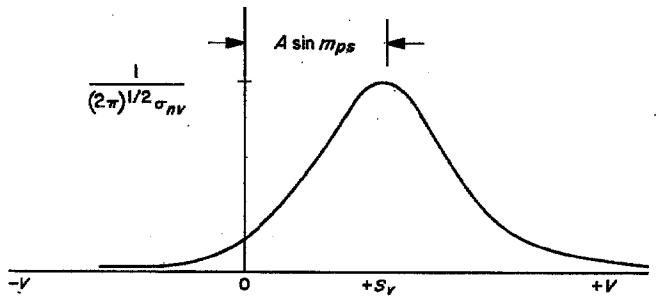


Fig. 12. Probability density function of observed voltage

Consider first a symbol period not preceded by a transition ($T_{SY_{11}}$ or $T_{SY_{00}}$). In particular, Fig. 13 shows a $T_{SY_{00}}$ type symbol period. The probability that the observed voltage V is greater than zero, given S_v, is represented by Expression (27). The $(S/N)_v$ is obtained from Expression (19) for time $t >> \tau_D$ and $m(t) = 1$.

$$P(V/S_v > 0) = \frac{1}{(2\pi)^{1/2}\,\sigma_{nv}} \int_0^{+\infty} \exp\left[-\tfrac{1}{2}\left(\frac{V - S_v^*}{\sigma_{nv}}\right)^2\right] dV \qquad (27)$$

where $V - S_v^* = N_v$ and N_v has rms amplitude σ_{nv}.

Expression (27) defines the probability that the observed voltage V is of the same polarity as the ideal or undistorted signal during a $T_{SY_{00}}$ symbol period. The expression is shown for a positive voltage symbol period.

[2]This provides maximum information rate (Ref. 1).

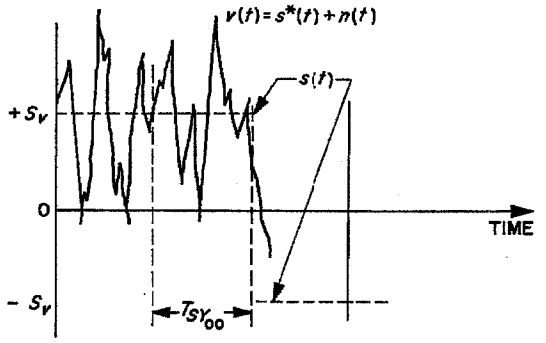


Fig. 13. Type $T_{SY_{00}}$ symbol period

For a negative voltage symbol period ($T_{SY_{11}}$), the probability that the observed voltage V is of the same polarity as the undistorted signal, given S_v, is

$$P[V/S_v < 0] = \frac{1}{(2\pi)^{1/2}\,\sigma_{nv}} \int_{-\infty}^{0} \exp\left[-\tfrac{1}{2}\left(\frac{+V - S_v^*}{\sigma_{nv}}\right)^2\right] dV \qquad (28)$$

(Note that S_v is negative in this case; therefore, the probability that V is also negative is the item of interest.) For the same $(S/N)_v$, the integrals in Expressions (27) and (28) are equal.

For a symbol period preceded by a data transition, as indicated in Fig. 14 for a $T_{SY_{10}}$ type symbol period, the time constant τ_D provides a time varying S_v^* during T_{SY} where $\tau_D/T_{SY} \leq 1/3$. In this case, the symbol period is divided into increments small enough so that, for all practical purposes, S_v^* can be considered constant during any one of these time increments. Expression (27) is evaluated at each increment to determine the probability that the observed voltage is of the same polarity as the ideal or

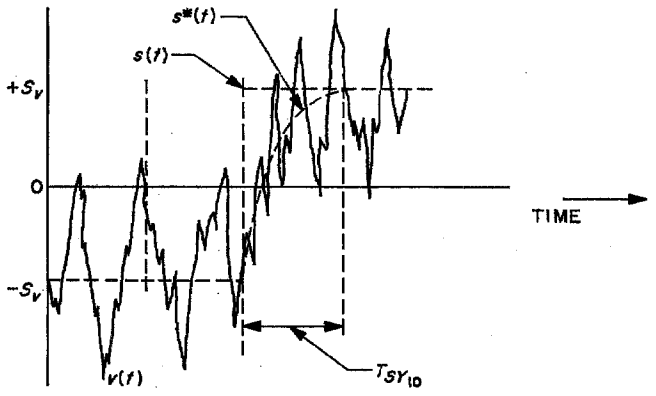


Fig. 14. Type $T_{SY_{10}}$ symbol period

undistorted signal. Note that the mean value S_v^* in each small time increment is not equal to S_v (Fig. 14). The $(S/N)_v$ is obtained from Expression (19) for each small increment of time starting at $t = 0$ and ending at $t = T_{SY}$. For a $T_{SY_{01}}$ type symbol period, Expression (28) is evaluated at each increment as described above.

The voltage at the output of the hard limiter which follows the data waveform filter assumes either of two states: $+1$ when $V > 0$ and -1 when $V < 0$, as indicated in Fig. 15. The output of the limiter represents the data symbol stream $m(t)$ with serrations due to noise plus a time delay at transitions due to the time constant τ_D. Designate the limiter output as an estimate of $m(t)$ or

$$\hat{m}(t) \tag{29}$$

The percentage of time that $\hat{m}(t)$ agrees with $m(t)$ can be obtained from Expressions (27) and (28) as an average over many digit periods. Note again that, for the $T_{SY_{10}}$ and $T_{SY_{01}}$ type symbol periods, this average is obtained for each of the small increments into which the symbol period was divided as described above. The overall average of all the small increment averages represents the percentage of time that $\hat{m}(t)$ agrees with $m(t)$ for these $T_{SY_{10}}$ and $T_{SY_{01}}$ periods. The assumption was made earlier that switching of the binary data signal was random with 50% probability that it does switch from one digit period to the next. This assumption will be altered later.

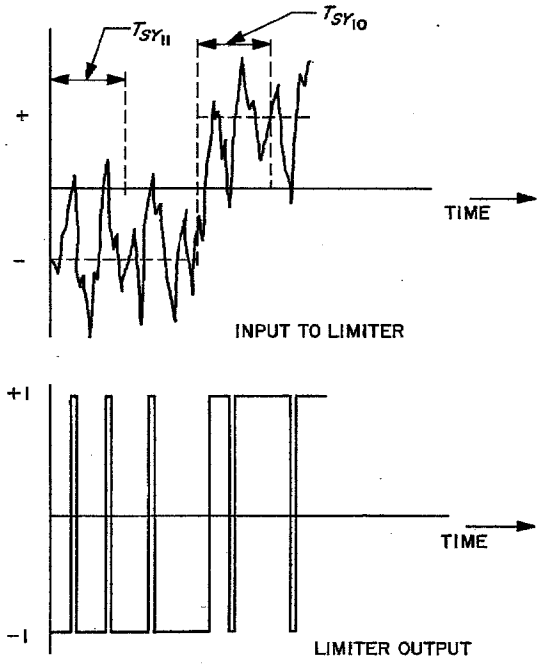


Fig. 15. Limiter input and output waveforms

The data symbol stream estimate $\hat{m}(t)$ biphase modulates the reference signal

$$(2)^{1/2} \sin(\omega_2 t) \tag{30}$$

plus and minus $\pi/2$ rad, which provides

$$\hat{m}(t)\,(2)^{1/2} \sin(\omega_2 t) \tag{31}$$

The output of the lower linear coherent amplitude detector in Fig. 6 is the detection of Expression (7) with reference signal ㉛ which provides (ignoring double frequency terms which are filtered out and the orthogonal terms)

$$m(t)\,\hat{m}(t)\,A \sin m_{ps} \{\cos[\omega_{sc} t + \theta] \times \sin[\omega_{sc} t + \hat{\theta}(t)]\} + n_{32}(t) \tag{32}$$

Assumption. *Since it is assumed the $\theta - \hat{\theta}(t)$ is much less than $\pi/2$ rad, the portion of the product of the square wave cosine and sine terms centered about dc is proportional to $[\theta - \hat{\theta}(t)]/(\pi/2)$ where the phase difference is expressed in radians.*

The other portion of the square wave cosine and sine product is a double frequency square wave which is filtered out by filter $F(s)$. It should be noted that the noise term $n_7(t)$ in Expression (7), which has a double sideband noise spectral density of $N_0/2$, is multiplied by $\hat{m}(t)$.

Assumption. *The assumption is made here that relative broadening of the noise spectrum due to this multiplication is small enough to be ignored. Consequently, the noise power represented by $n_{32}(t)$ is equal to $N_0/2 \times NBW_{F_{A2}}$. This is a conservative assumption. Note also that $\hat{m}(t)$ and the noise $n_7(t)$ are statistically independent, since the input noise is multiplied in the upper and lower input multipliers by orthogonal waveforms at the square wave subcarrier frequency (Fig. 6).*

From Expression (32), the error signal due to the signal alone out of the lower coherent amplitude detector is linearly related to the difference in phase between the received square wave telemetry subcarrier and the square wave subcarrier voltage-controlled oscillator. Its value is zero when θ and $\hat{\theta}(t)$ are equal, positive in sign when $\theta > \hat{\theta}(t)$, and negative in sign when $\theta < \hat{\theta}(t)$. The product $m(t)\,\hat{m}(t)$ is unity when $\hat{m}(t)$ is exactly $m(t)$. When $\hat{m}(t)$

does not agree with $m(t)$, the product $m(t)\hat{m}(t)$, when averaged over many symbol periods, is reduced. The average value of $m(t)\hat{m}(t)$ is shown in Expression (33)

$$\overline{m(t)\hat{m}(t)} = \begin{bmatrix}\text{fraction of time } \hat{m}(t) \text{ agrees with } m(t) \\ - \text{ fraction of time } \hat{m}(t) \text{ disagrees with } m(t)\end{bmatrix} \quad (33)$$

Consequently, $\overline{m(t)\hat{m}(t)}$ can be considered as a suppression factor which affects the phase error characteristic represented by the first term of Expression (32). Designate the suppression factor as α', then

$$\alpha' = \begin{bmatrix}\text{fraction of time } \hat{m}(t) \text{ agrees with } m(t) \\ - \text{ fraction of time } \hat{m}(t) \text{ disagrees with } m(t)\end{bmatrix} \quad (34)$$

The suppression factor α', Expression (34), is shown plotted in Fig. 16 as a function of ST_{SY}/N_0, the ratio of signal energy per symbol to noise spectral density. Note that if one bit of information transforms into l symbols and $ST_B/N_0 = y$ for the maximum permissible bit error rate (Ref. 2), then $ST_{SY}/N_0 = y/l$. ST_{SY}/N_0 can be rewritten as

$$\frac{S}{\frac{N_0}{2} \times \frac{2}{T_{SY}}}$$

If the above expression is related to Expression (19) when $t >> 1/(\beta T_{SY})$, where $\beta = \tau_D/(T_{SY})$ and $m(t) = \pm 1$, the following is observed by comparison of the numerators

$$(S)^{1/2} = A \sin m_{ps}$$

The denominator of Expression (19) can be written as

$$\left[\frac{1}{4\beta}\left(\frac{N_0}{2} \times \frac{2}{T_{SY}}\right)\right]^{1/2}$$

Consequently, for a given ST_{SY}/N_0 and τ_D/T_{SY}, the $(S/N)_v$ can be calculated from Expression (19) for any time t following a data transition. Supression factor (α') curves are shown for a 50% probability that the data symbol stream does switch from one symbol period to the next for ratios of τ_D/T_{SY} of 1/3, 1/6, and 1/12. Figure 16 also provides information for other distributions of zeros and ones in the data symbol stream. In particular, the suppression factor characteristic is shown for those cases when the probability is approaching 100 and 0%, respectively, that the data symbol stream does switch from one symbol period to the next (for ratios of τ_D/T_{SY} of 1/3, 1/6, and 1/12).

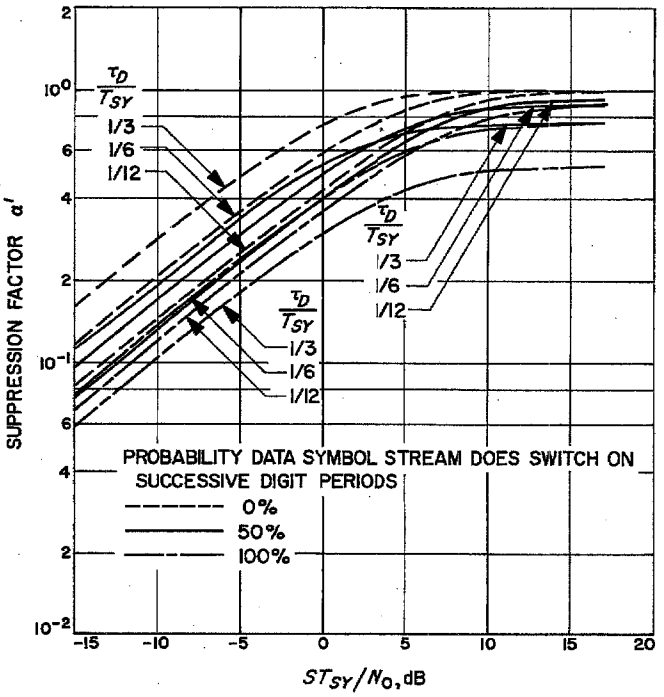


Fig. 16. MMTS subcarrier demodulator suppression factor versus ratio of signal energy per symbol to noise spectral density

Consider next the noise term $n_{32}(t)$ in Expression (32). The noise power represented by the noise term is

$$P_N = \frac{N_0}{2} \times NBW_{F_{A2}} \quad (35)$$

Since the noise is Gaussian, the variance of the noise is equal to the noise power

$$\sigma^2_{nv_2} = \frac{N_0}{2} \times NBW_{F_{A2}} \quad (36)$$

and, consequently, the rms noise voltage is

$$\sigma_{nv_2} = \left(\frac{N_0}{2} \times NBW_{F_{A2}}\right)^{1/2} \text{ rms amplitude} \quad (37)$$

Consider for a moment the signal portion of Expression (32). Note that if $\theta - \hat{\theta}(t)$ is equal to $\pi/2$ rad, the output voltage from the lower coherent amplitude detector is equal to $\alpha' A \sin m_{ps}$. Consequently, conversion of the rms noise voltage to equivalent phase noise can be accomplished by normalizing the noise voltage to the

signal voltage. The resultant expression at the output of the lower coherent amplitude detector is

$$\frac{\pi}{2} \times \frac{\sigma_{nv_2}}{\alpha' A \sin m_{ps}} \text{ rad rms}$$

or

$$\frac{\pi}{2} \times \frac{\left(\frac{N_0}{2}\right)^{1/2}}{\alpha' A \sin m_{ps}} \times (NBW_{F_{A2}})^{1/2} \text{ rad rms} \tag{38}$$

After passing through the filter $F(s)$, the signal plus noise represented by Expression (39) controls the output phase of the subcarrier VCO.

$$F(\omega)\,[\alpha' A \sin m_{ps}\,\{\cos[\omega_{sc}t + \theta] \times \sin[\omega_{sc}t + \hat{\theta}(t)]\} + n_{32}(t) \tag{39}$$

Since $\theta = \int \omega dt$, the VCO functions as an integrator.

Linear model of the subcarrier tracking loop. The lower loop in Fig. 6 can now be treated as a linear model of the phase-locked loop (Ref. 3) with the constraint that at minimum signal level the probability of the phase noise

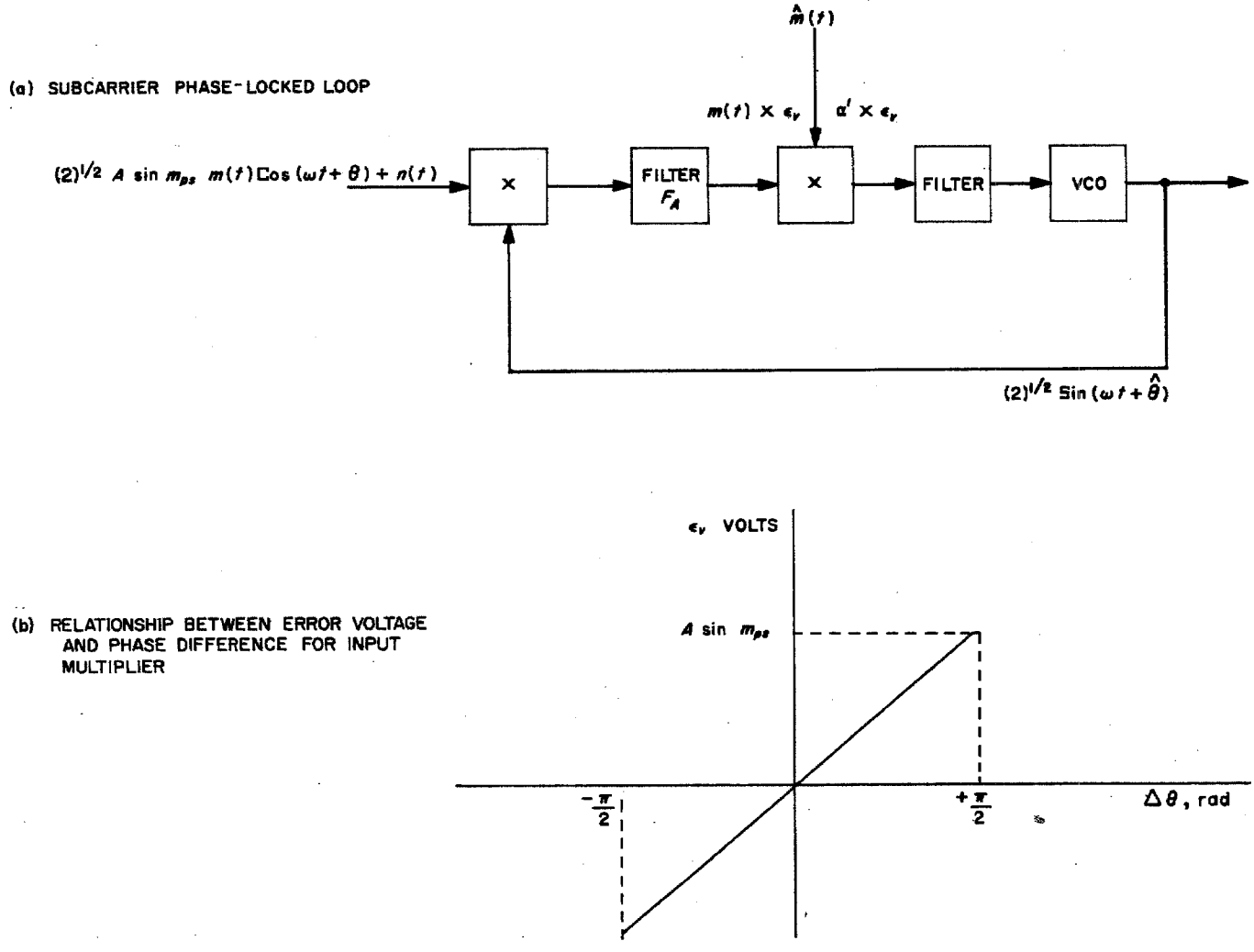


Fig. 17. Simplified block diagram of subcarrier phase-locked loop

error exceeding 90 deg $<<$ 1. Figure 12 shows a simplified tracking loop with an input signal

$$(2)^{1/2} A \sin m_{ps}\, m(t) \cos(\omega t + \theta) + n(t) \tag{40}$$

and an output signal

$$(2)^{1/2} \sin(\omega t + \theta) \tag{41}$$

The assumption is made that conversion of receiver noise to subcarrier phase noise is accomplished with essentially zero correlation between the two.

Also shown in Fig. 17 is the linear relationship between error voltage (ε_v) and phase difference ($\Delta\theta$) as produced by the input multiplier (assuming $m(t)$ is a constant for the moment). As described earlier (Fig. 2), the input noise has a two-sided noise spectral density of $S_N(f) = N_0/2$ in units of noise power per Hz. Since the linear input multiplier changes the input noise voltage $n(t)$ to noise voltage at its output that has the effect of phase noise, the input noise $n(t)$ can be replaced by an equivalent input phase noise $\theta_n(t)$. This equivalent input phase noise $\theta_n(t)$ will have a spectral density $S_{\theta n}(f)$ which can be expressed in units of rad²/Hz; which is flat, since the input noise voltage has a flat spectral density. If $m(t)$ is now considered a function of time and $\hat{m}(t)$ is an estimate of $m(t)$, the linear relationship between error voltage (ε_v) and phase difference ($\Delta\theta$) is modified by $\alpha' = m(t)\,\hat{m}(t)$ which was developed earlier (Fig. 11 and Expression (34)). Consequently, at the output of the second multiplier in Fig. 17, the slope of the ε_v vs $\Delta\theta$ linear characteristic varies with α' to provide a family of linear curves.

As developed earlier in Expression (32), the ε_v due to the signal is related to the phase difference by

$$\varepsilon_{v_s} = \frac{2}{\pi} \alpha' A \sin m_{ps} \times \Delta\theta \tag{42}$$

where $(2/\pi)\,\alpha' A \sin m_{ps}$ is expressed in units of volts per radian and $\Delta\theta$ in radians. The spectral density of the ε_v due to noise is related to the input noise spectral density by (see Expression 36)

$$S_{\varepsilon_N} = 1 \times \frac{N_0}{2} \text{ noise power per Hz} \tag{43}$$

Consequently, the noise spectral density of the equivalent input phase noise $\theta_n(t)$ is from Expressions (42) and (43)

$$S_{\theta n}(\omega) = \frac{\frac{N_0}{2}}{\left(\frac{2}{\pi} \alpha' A \sin m_{ps}\right)^2} \text{ rad}^2/\text{Hz} \tag{44}$$

The expression for $\theta_n(t)$ can now be written as

$$\theta_n(t) = \frac{n(t)}{\frac{2}{\pi} \alpha' A \sin m_{ps}} \tag{45}$$

In light of the development above, the subcarrier phase-locked loop can now be represented by the equivalent block diagram shown in Fig. 18. The multipliers shown in

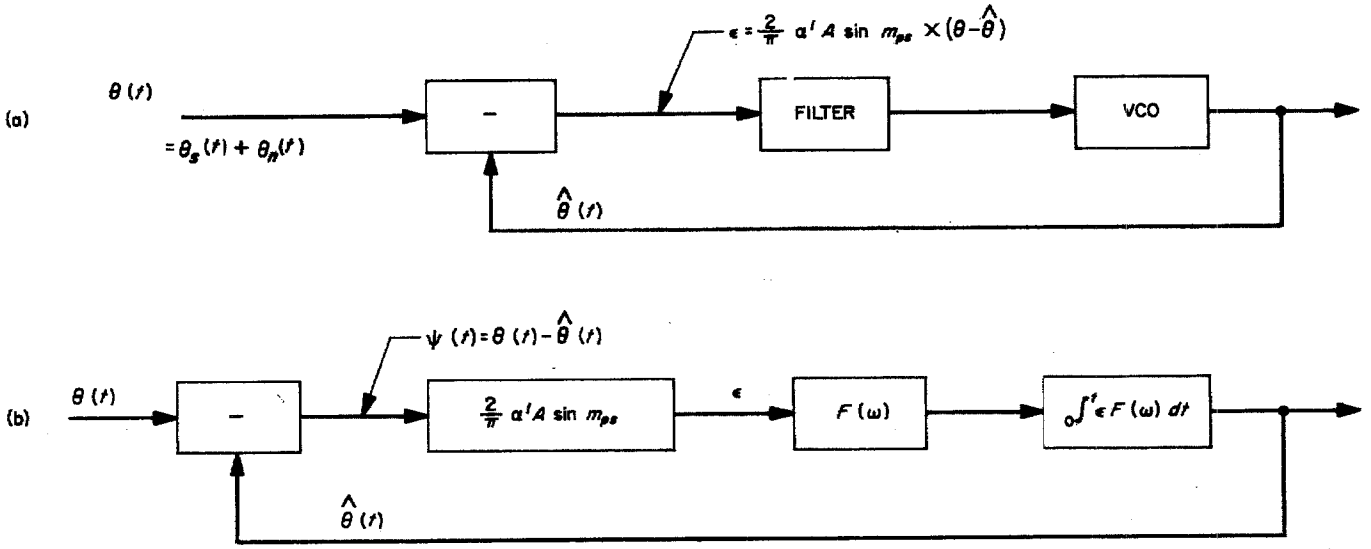


Fig. 18. Equivalent block diagram of subcarrier phase-locked loop

Fig. 17 are replaced by a phase differencing junction in Fig. 18. Figure 18(a) consists of a differencing junction, filter, and square-wave VCO. Figure 18(a) can be further represented by the equivalent block diagram shown in Fig. 18(b). Since the square-wave VCO functions as an integrator to produce the proper output phase, it is represented as

$$\int_0^t \varepsilon F(\omega)\, dt$$

in Fig. 18(b). The phase error is

$$\psi(t) = \theta(t) - \hat{\theta}(t) \tag{46}$$

Applying Laplace transform notation to Fig. 18(b), the linear model of the subcarrier phase-tracking loop becomes the model shown in Fig. 19. The subcarrier square-wave VCO becomes K/s in this mathematical model, where K is the effective gain constant of the VCO in radians per second per volt. Note that the open loop gain at dc is $(2/\pi) K \alpha' A \sin m_{ps}$. Referring to Fig. 19,

$$\hat{\theta}(s) = \frac{2}{\pi} K \alpha' A \sin m_{ps} \times \frac{F(s)}{s} \times [\theta(s) - \hat{\theta}(s)] \tag{47}$$

which becomes, after rearranging terms,

$$\hat{\theta}(s) = \frac{\frac{2}{\pi} K \alpha' A \sin m_{ps} \times F(s)}{s + \frac{2}{\pi} K \alpha' A \sin m_{ps} \times F(s)} \times \theta(s) \tag{48}$$

The transfer function of the subcarrier loop is from Expression (48)

$$H(s) = \frac{\hat{\theta}(s)}{\theta(s)} = \frac{\frac{2}{\pi} K \alpha' A \sin m_{ps} \times F(s)}{s + \frac{2}{\pi} K \alpha' A \sin m_{ps} \times F(s)} \tag{49}$$

Expression (48) provides a relationship which permits determination of an output phase function for a given input signal phase function. However, the equivalent input phase noise cannot be handled in this manner, since Laplace transforms do not, in general, exist for random processes. The noise spectral density of the equivalent input phase noise has been developed in Expression (44). Since the input noise is Gaussian and white,

$$P_N = \sigma_{\theta n}^2 = S_{\theta n}(\omega)\, BW_{SCL} \text{ rad}^2 \tag{50}$$

In addition, for linear filtering (Ref. 2)

$$P_N = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |H(j\omega)|^2 S_{\theta n}(\omega)\, d\omega \tag{51}$$

which can be expressed as

$$P_N = S_{\phi n}(\omega) \times \frac{1}{2\pi} \int_{-\infty}^{+\infty} |H(j\omega)|^2\, d\omega \tag{52}$$

Consequently, the two-sided noise bandwidth of the subcarrier phase-tracking loop is from Expressions (50) and (52)

$$BW_{SCL} = \frac{1}{2\pi} \int_{-\infty}^{+\infty} |H(j\omega)|^2\, d\omega \quad \text{Hz} \tag{53}$$

or, in Laplace transform notation

$$BW_{SCL} = \frac{1}{2\pi j} \int_{-j\infty}^{+j\infty} |H(s)|^2\, ds \quad \text{Hz} \tag{54}$$

The variance of the phase noise at the output of the loop is from Expressions (44), (50), and (54)

$$\sigma_{\theta n}^2 = \frac{\frac{N_0}{2}}{\left(\frac{2}{\pi} \alpha' A \sin m_{ps}\right)^2} \times BW_{SCL} \quad \text{rad}^2 \tag{55}$$

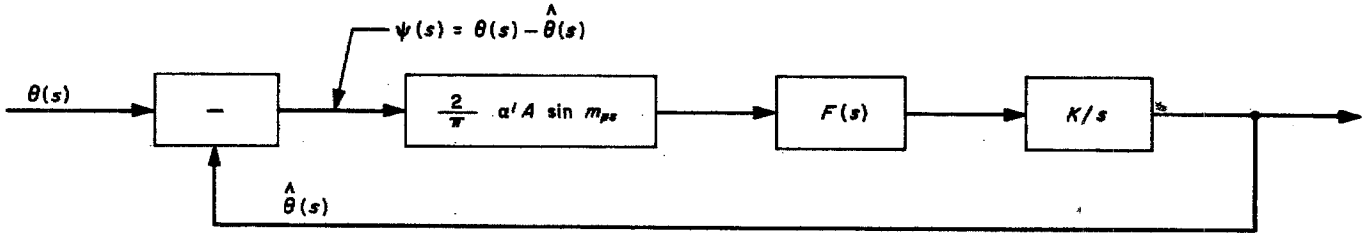


Fig. 19. Linear model of subcarrier phase-tracking loop

The square root of Expression (55) provides $\sigma_{\theta n}$, the rms phase noise at the output of the loop which, for a spectral line input signal, becomes the rms phase noise error in the loop.

First-order subcarrier tracking loop. Although the subcarrier demodulator loop may be designed as a second-order phase-locked loop, examination of the behavior of a first-order loop under noisy signal conditions will provide information on selection of closed-loop noise bandwidths for a large number of designs. The performance of a second-order loop under the same noisy signal conditions will be at least as good, if not better, than that of the first-order loop. The second-order loop will be considered in later reports.

For a first-order loop, $F(s) = 1$; therefore, from Expression (49), the transfer function becomes

$$H(s) = \frac{\frac{2}{\pi} K \alpha' A \sin m_{ps}}{s + \frac{2}{\pi} K \alpha' A \sin m_{ps}} \tag{56}$$

The two-sided closed-loop noise bandwidth is

$$BW_{SCL} = \frac{1}{2\pi} \int_{-\infty}^{+\infty} \frac{\left(\frac{2}{\pi} K \alpha' A \sin m_{ps}\right)^2}{\omega^2 + \left(\frac{2}{\pi} K \alpha' A \sin m_{ps}\right)^2} \, d\omega$$

$$= \frac{\left(\frac{2}{\pi} K \alpha' A \sin m_{ps}\right)}{2} \text{ Hz} \tag{57}$$

At the design point

$$BW_{SCL} = \frac{\alpha_0' \frac{2}{\pi} K A \sin m_{ps}}{2} \text{ Hz} \tag{58}$$

Since the two-sided noise bandwidth of a time constant τ is equal to $1/(2\pi)$ (from Expression 14), the equivalent time constant of the first-order loop is

$$\tau_L = \frac{1}{\alpha' \frac{2}{\pi} K A \sin m_{ps}} \tag{59}$$

Again, at the design point

$$\tau_{L0} = \frac{1}{\alpha_0' \frac{2}{\pi} K A \sin m_{ps}} \tag{60}$$

Note that the two-sided noise bandwidth is one half the reciprocal of the equivalent time constant of a first-order loop. Designate the ratio τ_{L0}, design point equivalent time constant, to T_{SY}, time duration of a symbol, as γ_0; then

$$\tau_{L0} = \gamma_0 T_{SY} \tag{61}$$

For a given design point, ST_{SY}/N_0, the variance of the phase noise at the output of the first-order loop at the design point is (from Expression 55):

$$\sigma_{\theta n}^2 = \left(\frac{1}{\alpha_0'}\right)^2 \left(\frac{\pi}{2}\right)^2 \times \frac{N_0}{ST_{SY}} \times \frac{T_{SY}}{2} \times \frac{1}{2\gamma_0 T_{SY}} \text{ rad}^2 \tag{62}$$

Now for a given τ_D/T_{SY}, γ_0, and probability that the data symbol stream does switch on successive symbols, the rms phase noise error at the design point can be calculated from Expression (62) where α_0' is obtained from Fig. 11. A change in ST_{SY}/N_0 from the design point provides an α' from Fig. 11 which provides, in turn, a new γ and $\sigma_{\theta n}^2$ is recalculated from the expression

$$\sigma_{\phi r}^2 = \left(\frac{1}{\alpha'}\right)^2 \left(\frac{\pi}{2}\right)^2 \times \frac{N_0}{ST_{SY}} \times \frac{1}{4\gamma} \text{ rad}^2 \tag{63}$$

Figure 20 shows the rms phase noise error $\sigma_{\theta n}$ for a first-order loop as a function of ST_{SY}/N_0 for τ_D/T_{SY} equal to 1/3 and 50% probability that the data symbol stream does switch on successive symbols. The design point is chosen for $ST_{SY}/N_0 = -10$ dB. Performance curves are shown for ratios of τ_{L0}/T_{SY} from 50 to 51,200 in octave steps. In general, the phase noise error $\sigma_{\theta n}$ should be maintained to 0.1 rad or less at the ST_{SY}/N_0 which provides a 10% bit error probability (Ref. 2) so as not to materially affect the signal-to-noise ratio of the detected data symbol stream. The effect of $\sigma_{\theta n}$ on the detected symbol stream will be presented in a later report.

b. Low- and medium-rate telemetry subcarrier demodulator. The low- and medium-rate telemetry subcarrier demodulator accommodates the engineering telemetry and nonvideo science data described in the introduction. Both of these data types are transmitted uncoded on a bit-by-bit basis which represents the condition $T_B = T_{SY}$ in the preceding general analysis.

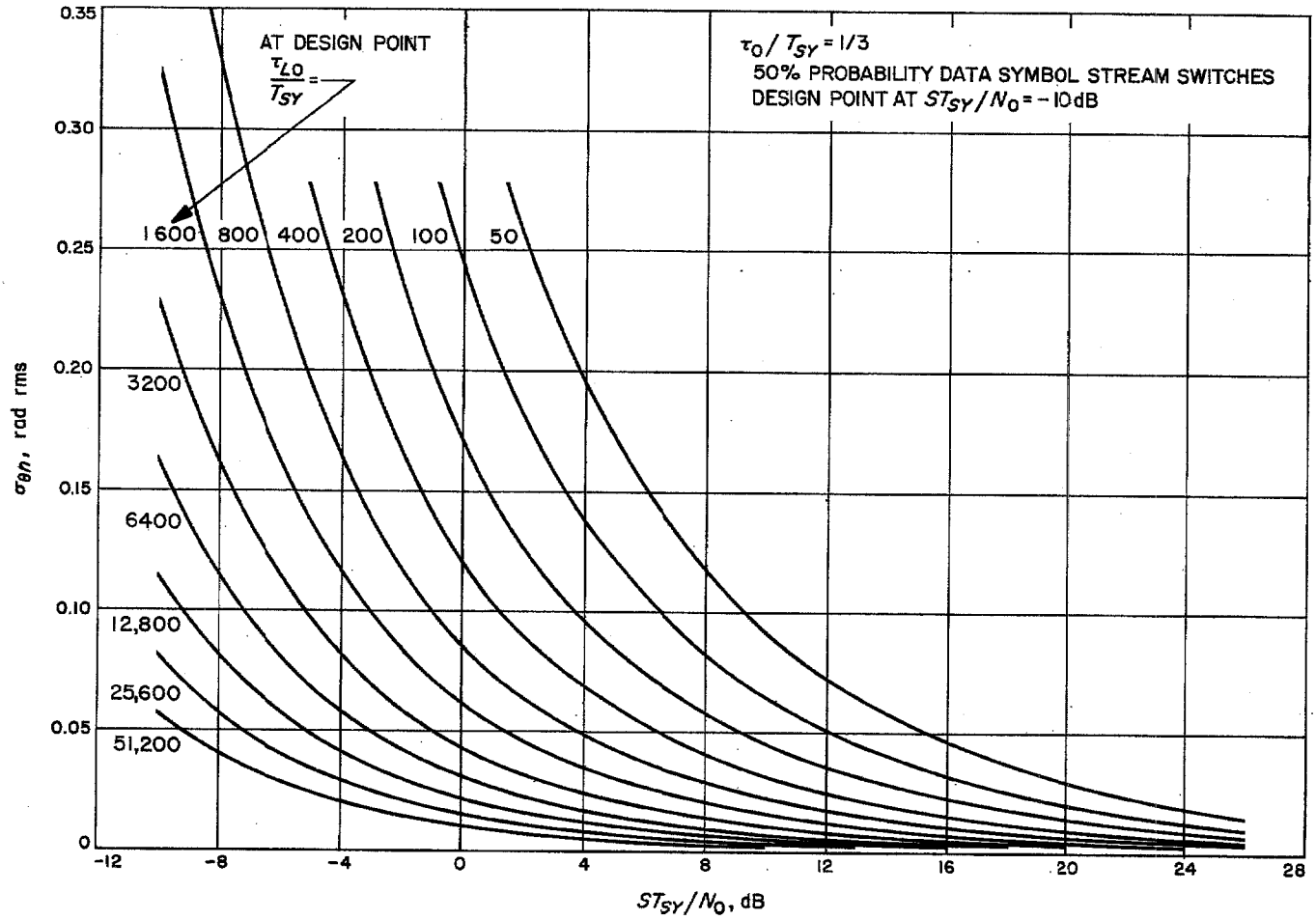


Fig. 20. MMTS subcarrier demodulator first-order loop rms phase noise error versus ratio of signal energy per symbol to noise spectral density

In order to apply the preceding analysis, consider the *Mariner* Mars 1969 mission as typical for a deep space mission. The nominal ST_B/N_0 for the overall telecommunications system design is +5.2 dB at encounter for low- and medium-rate data with a bit error rate of five parts in 10^3. The allowable degradation which is allocated to the telemetry subcarrier demodulator at this ST_B/N_0 of +5 dB is 0.1 dB. A degradation of 0.1 dB in the demodulated output ST_{SY}/N_0 due to the rms phase noise error in the subcarrier tracking loop results when $\sigma_{\theta n} = 0.02$ rad rms. In general, for the subcarrier demodulator

$$\frac{\text{demodulated } \frac{ST_{SY}}{N_0}}{\text{input } \frac{ST_{SY}}{N_0}} = \left[1 - \left(\frac{2}{\pi}\right)^{3/2} \sigma_{\theta n}\right]^2 \qquad (64)$$

where $3\sigma_{\theta n} \leq \pi/2$ and ST_{SY}/N_0 is expressed as a ratio. Derivation of this expression will be presented in a later report.

From Fig. 20 the curve for $\tau_{L0}/T_{SY} = 3200$ provides an rms phase noise error $\sigma_{\theta n}$ of 0.02 rad rms at an ST_{SY}/N_0 of +5.2 dB. At an ST_{SY}/N_0 of −1 dB which represents a 10% bit error rate (Ref. 2), $\sigma_{\theta n} = 0.05$ rad rms for the $\tau_{L0}/T_{SY} = 3200$ curve. Make this the design point for the low- and medium-rate telemetry. This provides from Expressions (58), (59) and (60) and from Fig. 16 a design point noise bandwidth of

$$BW_{SCL} = \frac{1}{2 \times 3200\, T_{SY}} \times \frac{0.490}{0.193} = \frac{1}{2520\, T_{SY}} \qquad (65)$$

to meet the requirements relative to phase noise error. Design point two-sided noise bandwidth is shown in Fig. 21 as a function of data rate. The noise bandwidth curve shown is for τ_D/T_{SY} equal to ⅓ with a 50% probability that the data stream switches from one bit period to the next. Changing τ_D/T_{SY} to ⅙ with all other conditions the same would reduce the noise bandwidth at any given data rate to 0.9 of that shown in Fig. 21. It should be noted that the subcarrier tracking loop if designed as a second-order loop would result in less than 0.02 rad rms noise error at ST_{SY}/N_0 equal to +5.2 dB. Also, the combined short-term stability of the square-wave telemetry subcarrier oscillator in the spacecraft and the square-wave subcarrier VCO in the DSN ground equipment must be such as to produce a phase error due to oscillator noise which is small compared to 0.05 rad rms in the design point noise bandwidth; for example, 0.015 rad rms.

The telemetry subcarrier demodulator must have sufficient open-loop gain and a maximum closed noise bandwidth capability to accommodate the doppler shift and doppler rate which occurs at injection of the spacecraft on its trajectory. Performance in this respect should be comparable to the RF system. Consider first the problem of accommodating doppler shift. The strong signal open-loop gain ($\alpha' = 1$) versus subcarrier frequency characteristic shown in Fig. 22 is obtained under the constraint that the phase error due to a frequency offset of 4.5 parts in 10^5 shall not exceed 0.1 rad at strong signal levels.

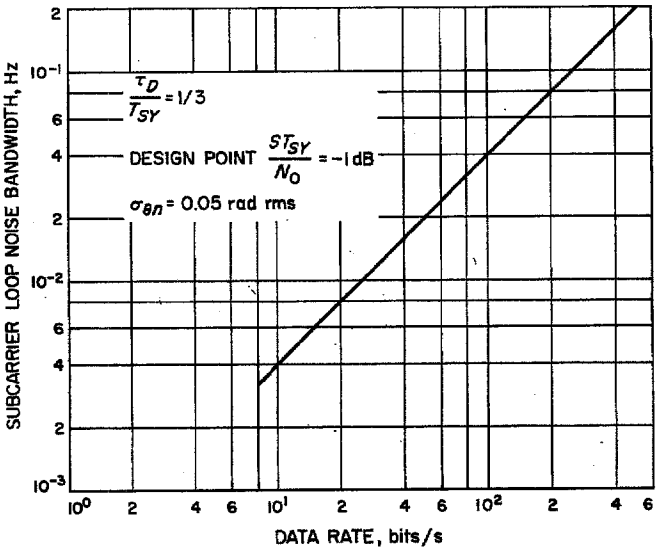


Fig. 21. Low- and medium-rate telemetry demodulator minimum design point noise bandwidth versus data rate

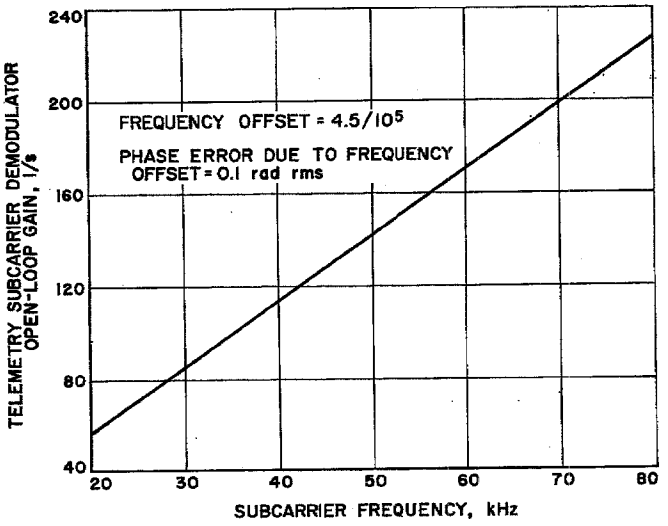


Fig. 22. Low- and medium-rate telemetry demodulator strong signal open-loop gain versus telemetry subcarrier frequency

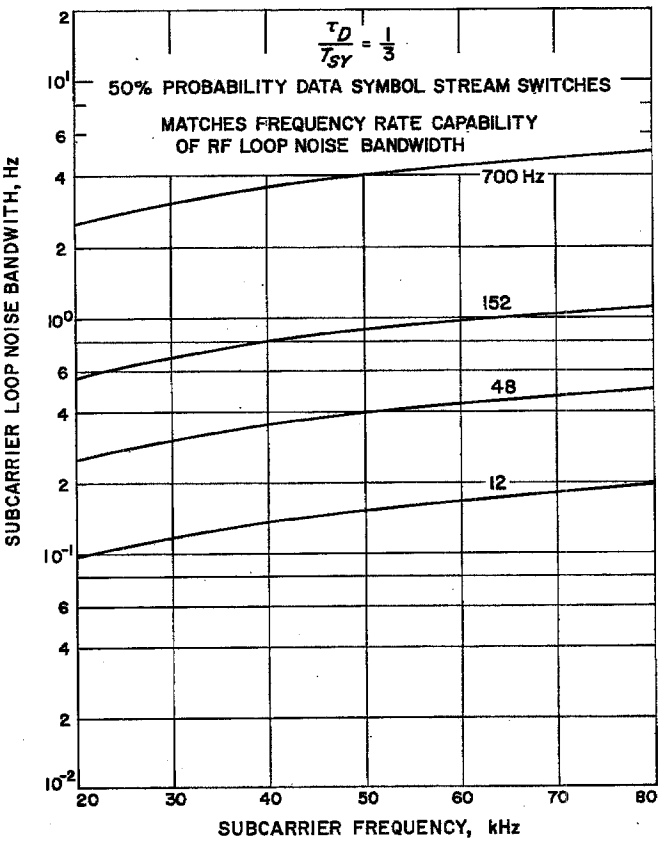


Fig. 23. Low- and medium-rate telemetry demodulator maximum design point noise bandwidth versus telemetry subcarrier frequency

Consider next the maximum design point two-sided noise bandwidth required to provide doppler rate tracking capability commensurate with the RF carrier tracking loop design point two-sided noise bandwidths of 12, 48, 152 and 700 Hz. This characteristic is shown in Fig. 23 as a function of subcarrier frequency. The 700-Hz RF carrier tracking bandwidth accommodates worst-case doppler rates during injection of the spacecraft on its mission trajectory. Figure 23 provides information on the maximum subcarrier design point noise bandwidth which matches the frequency rate capability of the RF carrier tracking system. The characteristic shown in Fig. 23 assumes that the subcarrier tracking loop is designed as a second-order loop with a damping factor of 0.707 at the design point.

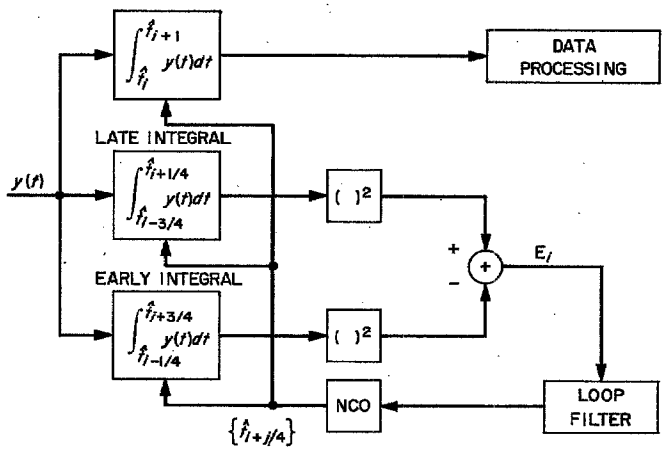


Fig. 24. Functional diagram of bit-timing subsystem

4. Telemetry Bit Synchronization Loop, *J. W. Layland*

a. General discussion. Bit synchronization for the MMTS must be obtained directly from the data signal. The methods by which this may be accomplished fall into two general categories: (1) The data signal is filtered, or processed nonlinearly and then filtered, to extract a frequency component which is a small ratio harmonic of the bit rate and coherent with the data stream. This frequency component is then tracked by a phase-locked loop to produce the bit-timing reference signal. (2) A bit-time tracking error signal is derived directly from the probabilistic transitions of the data signal, much as a range-code delay-locked loop error signal is derived from the known transitions of the pseudonoise ranging signal (Ref. 4). It is from this second category that the bit-tracking algorithm for the MMTS has been chosen.

The MMTS bit-tracking loop is functionally diagrammed in Fig. 24. An error signal is generated by differencing the squares of integrals of $y(t)$—the bit stream plus noise—each taken over a bit duration starting one-quarter bit time early and one-quarter bit time late; its operation is as follows:

Let t_i denote the actual epoch of the transition prior to the ith data bit and let $\hat{t}_i$ denote the local estimate of it. Assume that $y(t) = +1$ for $t \leq t_i$ and $y(t) = -1$ for $t > t_i$. Assume further that the numerically controlled oscillator (digital phase shifter) is out of phase such that $\hat{t}_{i+1/4} = t_i$. Then the late integral argument is $+1$ for the entire range; the early integral argument is $+1$ for the first half of its range and -1 for the second half of its range. As a result, the difference-of-squares error signal E_i is $+1 \cdot T_B^2$, where T_B is bit duration. If $-y(t)$ is substituted for $y(t)$, the same error signal is obtained. Consider now that the numerically controlled oscillator (NCO) is out of phase in the opposite direction by $T_B/4$, such that $\hat{t}_{i-1/4} = t_i$. Then the late integral argument is $+1$ for half of the range and -1 for the second half, giving a zero result. The early integral, however, has a -1 argument over the full range, producing an E_i of $-1 \cdot T_B^2$. Again, changing the sign of $y(t)$ does not change the error signal.

If now $\hat{t}_i$ is equal to t_i, the late integral argument is $+1$ for three fourths of the range and -1 for one fourth of the range, a net value of $T_B/2$. The early integral argument is $+1$ for ¼ the range and -1 for ¾ the range, for a net value of $-T_B/2$. The difference-of-squares error signal is zero. Similarly, if $y(t)$ has no transition in the range $\hat{t}_{i-3/4}$ to $\hat{t}_{i+3/4}$, the early and late integrals have identical values and the error signal is zero.

The error signal, then, depends only upon the relative positions of the transition time t_i and the estimate of it, $\hat{t}_i$. It does not depend upon the sign of the data transition, and is therefore a valid error signal to use for tracking data transitions which necessarily occur with random signs and interspersed with nontransitions.

b. Analysis of a first-order linear bit-tracking loop. The relative positions of timing marks for the early, late, and data integrations are shown in Fig. 25. Some simplifications, both in analysis and in computer implementation, may be obtained by reference to the labeling on the bottom line of Fig. 25. The late integral in the vicinity of

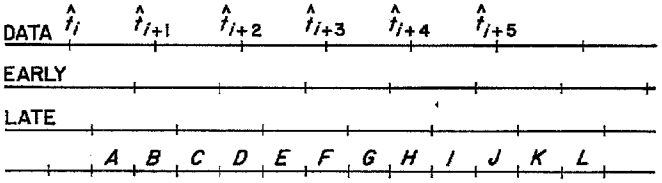


Fig. 25. Time points defining early, late, and data integrals

t_{i+2} is the sum of integrals C and D. The early integral there is $D + E$. The error signal at t_{i+2} is then

$$E_{i+2} = (C + D)^2 - (D + E)^2 = C^2 + 2D(C - E) - E^2 \quad (1)$$

Furthermore, breaking up the adjacent error signals shows

$$E_{i+1} = A^2 + 2B(A - C) - C^2$$
$$E_{i+3} = E^2 + 2F(E - G) - G^2 \quad (2)$$

Clearly, if the loop filter averages over a large number of bits—as it should—the squared terms drop, and only cross-terms remain at the input to the NCO. Figure 26 shows the reduced bit-timing subsystem. The analysis which follows for it produced results identical to the results obtained by a much more complicated route for the system of Fig. 24.

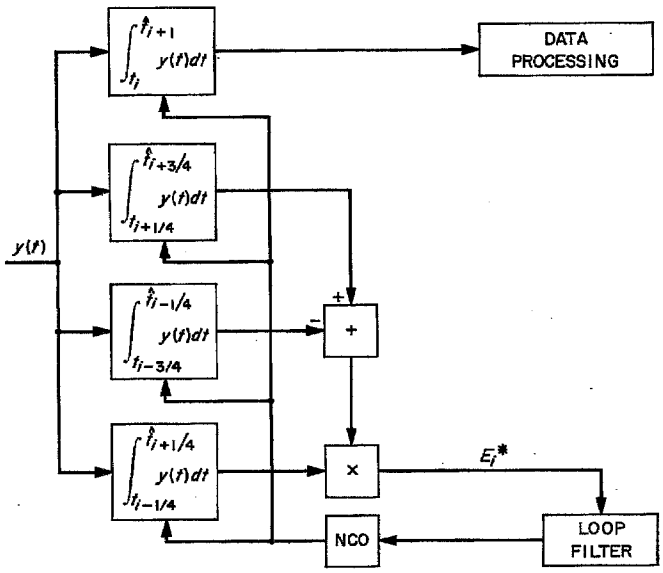


Fig. 26. Reduced bit-timing system

Let the input signal be normalized such that both the mean and variance of the integral of the signal-plus-noise over a bit time are given by $\rho^2 = 2ST_B/N_0$, where S is signal power, T_B is bit duration, and N_0 is the one-sided noise spectral density. Then the integrals, $I_{i,j}$, $j = 1, 2, 3$, which comprise the ith timing error sample, E_i^*, are given by

$$I_{i,1} = \int_{\hat{t}_{i+¼}}^{\hat{t}_{i+¾}} y(\tau)\,d\tau = M_i \frac{ST}{N_0} + n_1 \left(\frac{ST}{N_0}\right)^{½}$$

$$I_{i,2} = \int_{\hat{t}_{i-¼}}^{\hat{t}_{i+¼}} y(\tau)\,d\tau \quad (3)$$
$$= 2\frac{ST}{N_0}\left[M_{i-1}\left(\frac{1}{4} + \tau\right) + M_i\left(\frac{1}{4} - \tau\right)\right] + n_2\left(\frac{ST}{N_0}\right)^{½}$$

$$I_{i,3} = \int_{t_{i-¾}}^{t_{i-¼}} y(\tau)\,d\tau = M_{i-1}\frac{ST}{N_0} + n_3\left(\frac{ST}{N_0}\right)^{½}$$

where n_1, n_2, n_3 are mutually independent zero-mean, unit variance Gaussian random variables, M_i and M_{i-1} are the values ($+1$ or -1) of the ith and $i-1$th data bits, and τ is the timing error—in fractions of the bit duration. T_B—between the (possible) transition time t_i and the estimate of it, $\hat{t}_i$. The ith timing error sample, E_i^*, and the expected value of it, $\overline{E_i^*}$, are given in Eq. (4)

$$E_i^* = I_{i,2}^*(I_{i,3} - I_{i,1})$$
$$= 2\left(\frac{ST}{N_0}\right)^2 (M_{i-1} - M_i)\left(M_{i-1}\left[\frac{1}{4} + \tau\right] + M_i\left[\frac{1}{4} - \tau\right]\right)$$
$$+ \text{noise terms} \quad (4)$$

$$\overline{E_i^*} = \left(\frac{ST}{N_0}\right)^2 \left\{2\tau(M_{i-1} - M_i)^2 + \frac{1}{2}(M_{i-1}^2 - M_i^2)\right\}$$
$$= 0, \qquad \text{if } M_i = M_{i-1}$$
$$= 8\tau\left(\frac{ST}{N_0}\right)^2, \qquad \text{if } M_i \neq M_{i-1}$$

The noise terms not explicitly shown in Eq. (4) will produce a jitter in the resulting time estimate from the NCO, and thus cannot be ignored. The mean-squared value of E_i^* is given by

$$\overline{E_i^{*2}} = \overline{E_i^*}^2 + \left(\frac{ST}{N_0}\right)^3 (M_i - M_{i-1})^2 + 2\left(\frac{ST}{N_0}\right)^2$$
$$+ 8\left(\frac{ST}{N_0}\right)^3 \left[M_{i-1}\left(\frac{1}{4} + \tau\right) + M_i\left(\frac{1}{4} - \tau\right)\right]^2 \quad (5)$$

Furthermore, $I_{i,1}$ is identical to $I_{i-1,3}$ and $I_{i,3}$ is identical to $I_{i+1,1}$, so each of these is used in producing the $i-1$th and the $i+1$th error sample, respectively. The cross-correlations with adjacent error samples are given by

$$\overline{E_{i+1} \cdot E_i} = \overline{E_i} \cdot \overline{E_{i+1}} - 4\left(\frac{ST}{N_0}\right)^3 \times \left(\frac{M_i + M_{i-1}}{4} - \tau\,[M_i - M_{i-1}]\right) \times \left(\frac{M_{i+1} + M_i}{4} - \tau\,[M_{i+1} - M_i]\right) \tag{6}$$

$$\overline{E_{i-1} \cdot E_i} = \overline{E_i} \cdot \overline{E_{i-1}} - 4\left(\frac{ST}{N_0}\right)^3 \times \left(\frac{M_i + M_{i-1}}{4} - \tau\,[M_i - M_{i-1}]\right) \times \left(\frac{M_{i-2} + M_{i-1}}{4} - \tau\,[M_{i-1} - M_{i-2}]\right)$$

E_i is not correlated with timing error samples not adjacent to it. Since the loop filter averages over a large number of error signals, the effective variance of E_i is given by

$$V_{eff}\{E_i\} = \overline{E_i \cdot E_i} - \overline{E_i}^2 + \overline{E_i E_{i+1}} - \overline{E_i}\,\overline{E_{i+1}} + \overline{E_i E_{i-1}} - \overline{E_i}\,\overline{E_{i-1}} \tag{7}$$

and if $\tau \approx 0$, the effective variance reduces to

$$V_{eff}\{E_i\} = 2\left(\frac{ST}{N_0}\right)^2 + \left(\frac{ST}{N_0}\right)^3, \quad \text{if } M_i M_{i-1} = 1$$
$$= 2\left(\frac{ST}{N_0}\right)^2 + 4\left(\frac{ST}{N_0}\right)^3, \quad \text{if } M_i M_{i-1} = -1 \tag{8}$$

Software timing constraints may make it desirable not to generate a bit-timing sample for every possible transition. If this is done, the correlation for adjacent error samples does not exist, and the effective variance of E_i is

$$V_D\{E_i\} = 2\left(\frac{ST}{N_0}\right)^2 + 2\left(\frac{ST}{N_0}\right)^3, \quad \text{if } M_i M_{i-1} = 1$$
$$= 2\left(\frac{ST}{N_0}\right)^2 + 4\left(\frac{ST}{N_0}\right)^3, \quad \text{if } M_i M_{i-1} = -1 \tag{9}$$

To consider the E_i in the delay-locked loop, normalize the signal such that

$$\overline{E_i} = \tau, \qquad \tau \text{ for } |\tau| \leq \frac{1}{4}$$

or

$$\overline{E_i} = 0, \quad \text{if } M_i M_{i-1} = 1$$
$$= 2\tau, \quad \text{if } M_i M_{i-1} = -1 \tag{10}$$

Then the effective variance of the ith sample becomes

$$V_{Ei} = \frac{1}{8}\left(\frac{N_0}{ST}\right)^2 + \frac{1}{16}\left(\frac{N_0}{ST}\right), \quad \text{if } M_i M_{i-1} = 1$$
$$= \frac{1}{8}\left(\frac{N_0}{ST}\right)^2 + \frac{1}{4}\left(\frac{N_0}{ST}\right), \quad \text{if } M_i M_{i-1} = -1$$

Let X_i be the sequence of bit-time estimates and Z_i be the sequence of true bit times, and implement the delay-locked loop by the difference equation

$$X_{i+1} = X_i + K \cdot E_i \cong X_i + K \cdot (Z_i - X_i) \tag{11}$$

where E_i is the error signal generated by the method just described. To account for the randomness of the data stream, let $d_i = M_i M_{i-1}$ take values $+1$ and -1 with equal probability. The loop closure equation then becomes

$$X_{i+1} = X_i + K(1 + d_i)(Z_i - X_i) + K[N_{i1} + (1.5 + 0.5 d_i) N_{i2}] \tag{12}$$

where

$$\overline{N_{i1}} = \overline{N_{i2}} = \overline{N_{i1} N_{i2}} = 0$$

$$\overline{N_{i1}^2} = \frac{1}{8}\left(\frac{N_0}{ST}\right)^2$$

$$\overline{N_{i2}^2} = \frac{1}{16}\left(\frac{N_0}{ST}\right)$$

Assume that $Z_i = Z + i\psi$. Taking the expected value of the $\{X_i\}$ as given in Eq. (12), and assuming a steady-state solution produces

$$E\{X_i\} = Z_i - \frac{\psi}{K} \tag{13}$$

In a similar manner, the variance of the $\{X_i\}$ in steady state may be determined to be

$$V_x = V_x(\overline{1 + k[1 + d]})^2 + K^2[\overline{N_{i1}^2} + (\overline{1.5 + 0.5d})^2 + \overline{N_{i2}^2}] \quad (14)$$

$$V_x = \frac{K}{2(1-K)}\left[\frac{1}{8}\left(\frac{N_0}{ST}\right)^2 + \frac{5}{32}\left(\frac{N_0}{ST}\right)\right] \quad (15)$$

The development of V_x has assumed that the error signal is linear. In reality, symmetries between the integrations involved in Eq. (4) produce an error signal whose expected value is shown in Fig. 27. To verify Eq. (15), a Fortran simulation was run using $K_\tau = 0.005$, with excellent agreement with Eq. (15), as shown in Fig. 28. Figure 29 shows the error-rate data from the same simulation.

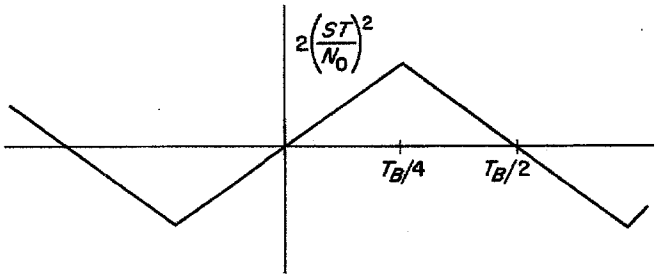


Fig. 27. Error signal of delay-lock loop

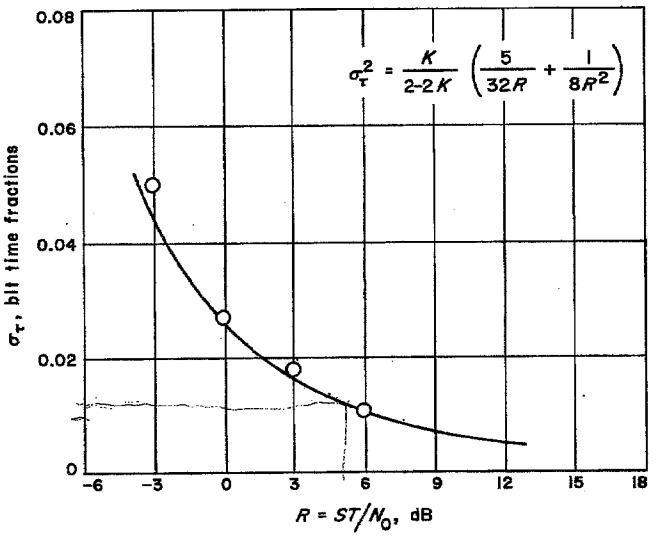


Fig. 28. Timing jitter—theoretical and simulation results for loop gain = 0.005

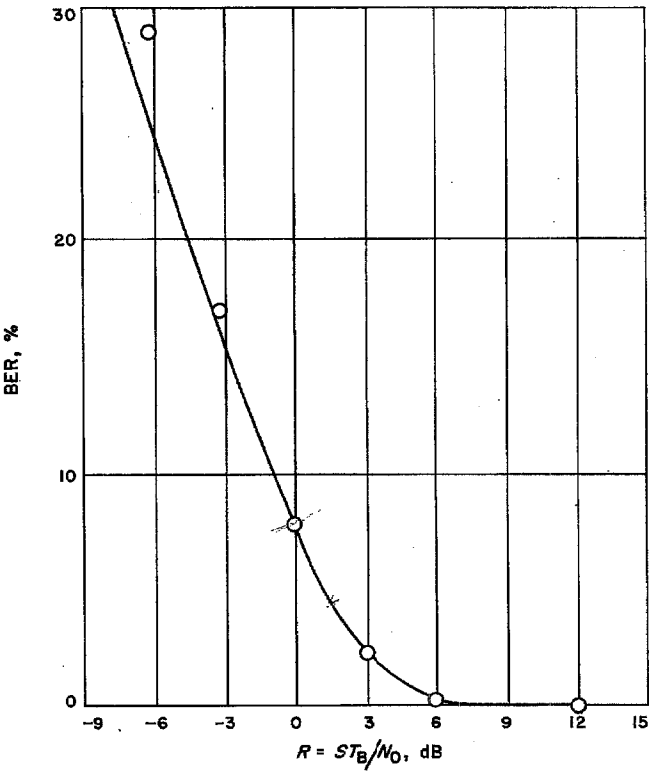


Fig. 29. Comparison of perfectly timed detection BER and simulated results for data-derived sync

Even though the individual error signals are not Gaussian, the timing sequence itself may be treated as if Gaussian with variance given by Eq. (15) for small K. The X_i represent, effectively, an average over $2/K$ of the past E_i, which converges to a Gaussian distribution as K decreases.

The degradation, if any, in bit-error probability due to bit-timing noise may be computed using this approximation to the distribution of the $\{X_i\}$.

c. Effects of bit sync jitter on detection. If the effects of the RF and subcarrier tracking loops are ignored, the effects of bit-timing jitter on the error probability of a correlation detector is a quite simple and well-documented phenomenon (Refs. 5 and 6). Figure 30 shows a possible data waveform, along with an erroneous sequence of estimated transition times and the resultant waveform in the correlation detector. It is evident that the timing offset, $\hat{t}_i - t_i$, has no effect on the correlator output unless a data transition is crossed. If a transition is crossed, the effective signal amplitude is reduced by a factor $(1 - 2|\tau|)$

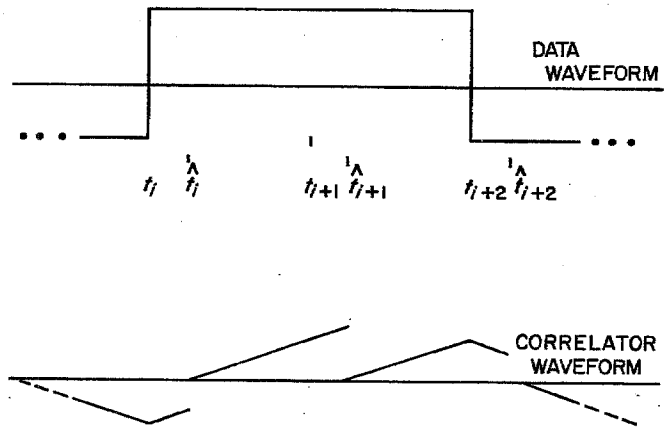


Fig. 30. Effects of bit-timing errors

where τ is the timing error measured in fractions of the bit duration. Since the probabilities of encountering a transition and a nontransition between any two bits may be assumed to be both equal to ½, the probability of bit-detection error is

$$P_e = \frac{1}{2}\int_{-\frac{1}{2}}^{\frac{1}{2}} p(\tau)\,\mathrm{erfc}\left(\left[\frac{2ST_B}{N_0}\right]^{\frac{1}{2}} x\,[1-2|\tau|]\right)d\tau + \frac{1}{2}\,\mathrm{erfc}\left(\frac{2ST_B}{N_0}\right)^{\frac{1}{2}} \tag{16}$$

where $\mathrm{erfc}(x)$ denotes the integral from x to ∞ of the standardized Gaussian density function and $p(\tau)$ is the probability density function of τ, the timing error.

Exact evaluation of Eq. (16) would require numerical integration, which is probably not justified without including the effects of the subcarrier loop in the distribution of τ. As an alternative, the effective signal-to-noise ratio (SNR) at the output of the data correlator may be computed. If this effective SNR is only slightly degraded by the timing jitter, the increase in error probability due to timing jitter will also be slight; but the nonlinearity of the $\mathrm{erfc}(x)$ function makes a more quantitative connection difficult. Nevertheless, the convenient degradation-in-SNR model will be used as a performance measure for the remainder of the bit-synchronizer discussion instead of the more exact but cumbersome bit error rate (BER) model as described by Eq. (16). This effective SNR is given by

$$SNR_E = \frac{ST_B}{N_0}\left[\frac{1}{2}\int_{-\frac{1}{2}}^{\frac{1}{2}} p(\tau)\,[1-2|\tau|]^2\,d\tau + \frac{1}{2}\right] \tag{17}$$

and if jitter is controlled to a small enough variance for the Gaussian approximation to be valid,

$$SNR_E \approx \frac{ST_B}{N_0}\left[1-2\left(\frac{2}{\pi}V_x\right)^{\frac{1}{2}}\right] \approx \frac{ST_B}{N_0}\left[1-2\left(\frac{K}{\pi(1-K)}\left[\frac{1}{8}\left(\frac{N_0}{ST_B}\right)^2 + \frac{5}{32}\left(\frac{N_0}{ST_B}\right)\right]\right)^{\frac{1}{2}}\right] \tag{18}$$

where the jitter variance in Eq. (15) has been used. The loss in SNR due to timing jitter is plotted in Fig. 31 as a function of ST_B/N_0 for several values of K, the bit-tracking loop gain.

d. The acquisition problem. When it is initially activated, the bit-synchronizer timing generator will produce marker pulses which are at the same rate as the received bits (to a close tolerance) but which have an unknown phase error with respect to the received data bits. Before the data can be reliably detected, this phase error must be reduced to a very small value. One way of doing this is simply to allow the bit-time tracking device to track to a stable node. This process, however, is slow; and at low bit rates may take many minutes. The acquisition procedure introduced and analyzed in the following section

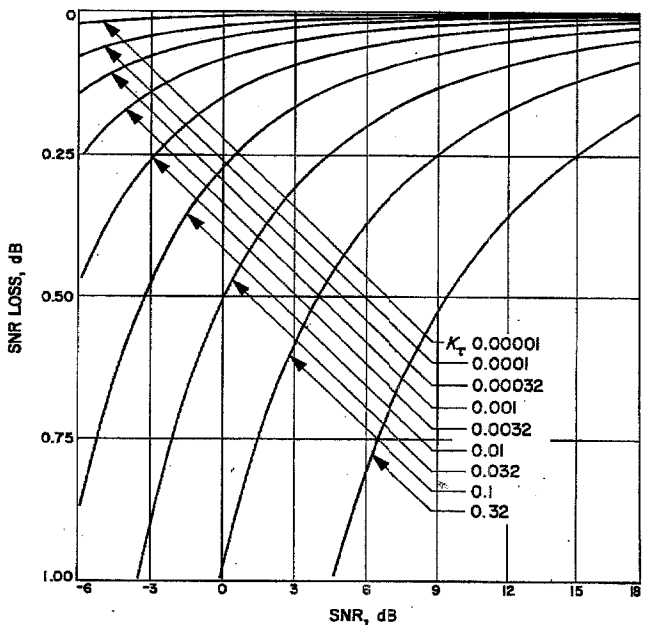


Fig. 31. SNR loss due to timing jitter

has the (possible) disadvantage that no data can be detected while acquisition proceeds, coupled with the advantage that both the acquired timing jitter and the probability of failure can be made as small as desired if there is no rate error between the received signal and the timing generator.

The acquisition process is functionally diagrammed in Fig. 32. The number-controlled oscillator (NCO) used in the bit-tracking process is initialized to run at the proper bit rate; and, as the data is received, the four y_j's are computed:

$$y_j = \sum_{i=1}^{N} \left(\int_{t_{i+j/4}}^{t_{i+1+j/4}} y(t)\, dt \right)^2, \qquad j = 0, 1, 2, 3 \tag{19}$$

where $y(t)$ is the received signal; N is the number of bits used in the acquisition process. The y_j's are differenced to form the δ_j $(j = 0, 1)$, which are used to compute τ, the delay shift from y_0's start to the true bit start time. The expected values of the δ_j are shown in Fig. 33. Let $E\{\delta_j\} = d_j$ $(j = 0, 1)$. The d_j's follow these rules:

$$\begin{aligned} &\text{If } d_0 > 0, && d_1 = A \cdot (4\tau) \\ &\text{If } d_0 \leq 0, && d_1 = A \cdot (2 - 4\tau) \\ &\text{If } d_1 > 0, && d_0 = A \cdot (1 - 4\tau) \\ &\text{If } d_1 \leq 0, && d_0 = A \cdot (4\tau - 3) \end{aligned} \tag{20}$$

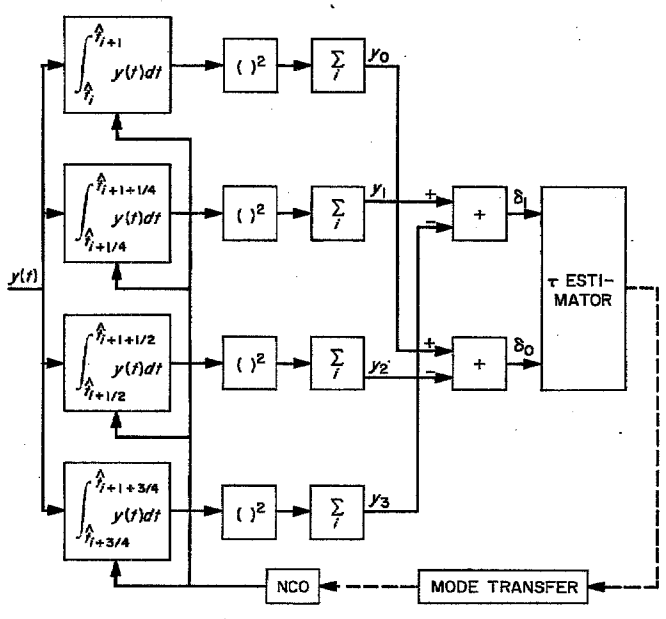


Fig. 32. Functional diagram of acquisition process

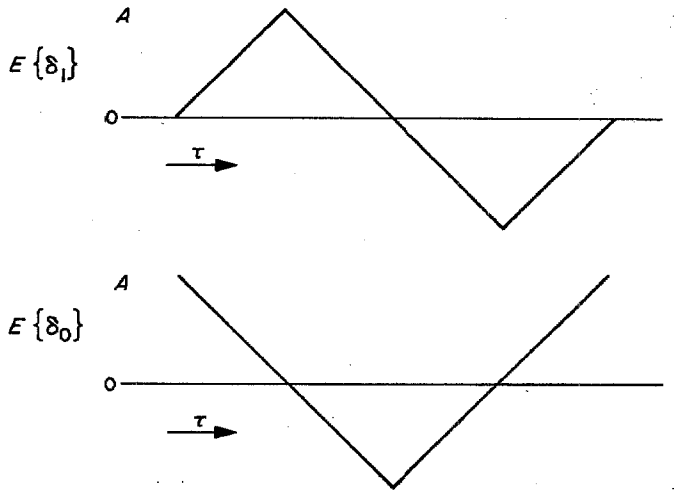


Fig. 33. Expected value of δ_j's as a function of τ

Either of the two δ_j's could be selected as a pivot and τ estimated using $\delta_{\bar{j}}$ and the proper equation from Eq. (20). The probability of the acquisition failure is the probability that the wrong sign is selected for the pivot δ_j, i.e.,

$$P_r\{\text{acq fail}\} = P_r\{d_j \cdot \delta_j < 0 \mid \delta_j \text{ is pivot}\} \tag{21}$$

Since choice of pivot is arbitrary, it should be selected to minimize (if possible) the failure probability. This can be done by selecting that δ_j which is larger in magnitude as the pivot. With this additional constraint

$$P_r\{\text{acq fail}\} = P_r\{(d_j \cdot \delta_j < 0) \cdot (|\delta_j| > |\delta_{\bar{j}}|)\} \tag{22}$$

Figure 34 shows the locus of d_j/d_j and the associated failure region in $\delta_j/\delta_{\bar{j}}$ space for τ in one particular quadrant of its range. Since the problem is symmetric, only one quadrant need be considered. The probability of failure is clearly bounded above by the probability of failure when the noises are fully correlated, or

$$P_r\{\text{acq fail}\} \leq P_r\left\{\delta_j < d_j - \frac{A}{2}\right\} \tag{23}$$

(d_j assumed positive). The statistics of the δ_j were determined in the first-order loop-tracking analysis.

Assume that M data transitions occurred in the signal used to generate the y_j's, and assume further that both N and M are large enough that end-effects in the summations may be ignored. Then it follows from Eqs. (4)

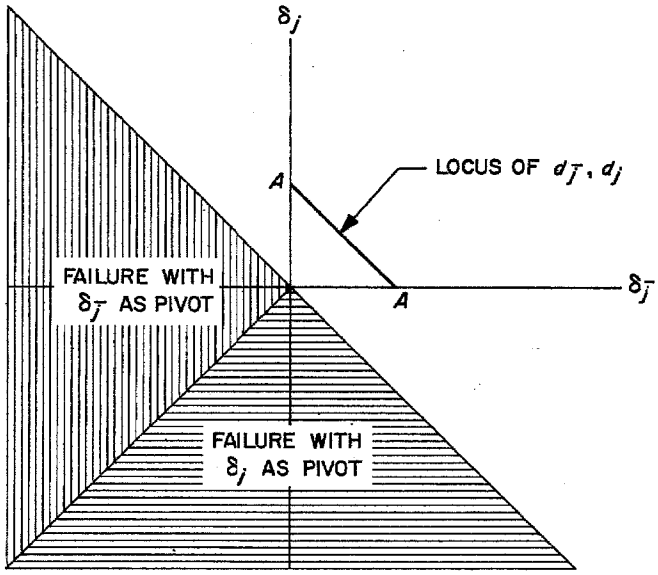


Fig. 34. Locus of d_j, $d_{\bar{j}}$ and the acquisition failure region for one quadrant of τ's range

and (6) that

$$E\{\delta_1\} = 2M\left(\frac{ST_B}{N_0}\right)^2 4\tau \tag{24}$$

$$V\{\delta_1\} = 2N\left(\frac{ST_B}{N_0}\right)^2 + M\left(\frac{ST_B}{N_0}\right)^3 \times\left[6 - 2\frac{M}{N} + 32\tau^2\left(1+\frac{M}{N}\right)\right]$$

for $|\tau| \leq \frac{1}{4}$. Equation (24) may be extended in the obvious manner to apply to δ_0 and to δ_1 with $|\frac{1}{2} - \tau| \leq \frac{1}{4}$. Applying Eq. (24) to Eq. (23), and taking an upper bound on the variance produces

$$P_\tau(\text{acq fail}) \leq P_r\left(N_1 > \frac{1}{\left[\frac{N}{2M^2R^2} + \frac{2}{MR}\right]^{1/2}}\right) \tag{25}$$

where N_1 is a zero-mean unit-variance Gaussian-random variable, and $R = ST_B/N_0$. If the data bits are assumed independent and $(^{+1}_{-1})$ equiprobable, the expected value of M is $N/2$. The bound in Eq. (25) is monotonically decreasing in N if M is proportional to N, and can be forced to assume as small a value as desired. One approach to specifying the acquisition process using Eq. (25) would be to set a threshold on M, e.g., $M_T = N/4$, and reject data if the measurements fell below that level. The proper value of N could then be specified from the acceptable failure probability level, and the SNR.

The failure probability is only one of the two parameters necessarily connected with the acquisition process. The other parameter of interest is the resultant jitter in the estimated τ. To invert Eq. (20), the parameter A must be known. From Eq. (24), $A = 2M(ST_B/N_0)^2$; and since M depends upon the data sequence, it must be estimated. Note from Fig. 33

$$|d_0| + |d_1| = A \tag{26}$$

Then if the SNR of the δ_j's is high

$$|\delta_0| + |\delta_1| \approx A \tag{27}$$

with high probability. Thus, if δ_0 is selected as the pivot, τ is in 1st or 4th quadrants, assuming no acquisition failure.

$$\hat{\tau} = \frac{\frac{1}{4}\delta_1}{|\delta_0| + |\delta_1|} \tag{28}$$

Let $\delta_1 = d_1 + n_1$, $|\delta_1| = |d_1| + n_1'$, $|\delta_0| = |d_0| + n_0'$

$$\hat{\tau} = \frac{1}{4}\frac{d_1 + n_1}{|d_1| + |d_0| + n_0' + n_1'} \tag{29}$$

$$\hat{\tau} = \tau + \frac{\frac{1}{4}n_1 - \tau n_1' - \tau n_0'}{|d_0| + |d_1|} + \text{higher order terms in } n_0', n_1'$$

If SNR is high, the higher-order terms in Eq. (29) may be neglected; and either the contribution of the n's may be neglected because τ is small, or they may be treated as Gaussian because the probability of their affecting the absolute value operation in Eq. (28) is small. In either case, the variance of $\hat{\tau}$ is given approximately by

$$V(\tau) \approx \frac{1}{8MR} + \frac{N}{32M^2R^2} \tag{30}$$

where again, the upper bound on the variance in Eq. (24) has been used. Interestingly enough, comparison of

Eqs. (25) and (30) reveals that

$$P_r\{\text{acq fail}\} \geqq P_r\left\{\tau - \tau > \frac{1}{4}\right\} \tag{31}$$

under the assumptions of this analysis.

One of the assumptions made throughout this analysis was that τ did not vary as the N bits entering into the δ_j were received. While this restriction is not completely necessary, the expected value of the final time estimate will be the average of the true τ, provided τ varies slowly and over a small range during reception of the block of N data bits. If, for example, a rate error of 10^{-4} bits/bit existed between the timing generator and the actual bit stream, there would be a 2% drift in τ over a block of 200 data bits, and a corresponding 1% systematic error in the estimated τ. In general, the value of N chosen for a particular application will be a compromise between this systematic error, on the one hand, and jitter and acquisition failure probability, on the other. This compromise is the same one which must be made between jitter and static phase error in a first-order tracking loop with ramp input.

e. Second-order loop filter. One way of eliminating the static phase error arising from tracking a ramp input is the use of a second-order tracking filter. Doppler nominally is on the order of 10^{-5} to 10^{-6} bits/bit, but anomalies in the data source can push this to perhaps 10^{-3} bits/bit, which would create a sizeable static timing error for a loop gain of 10^{-2} or less. For this reason, the succeeding paragraphs will explore a few of the properties of a second-order digital tracking filter.

Figure 35 is a functional diagram of the discrete second-order tracking filter. This filter is governed by the set of difference equations:

$$\begin{aligned} E_i &= Z_i - X_i \\ F_i &= F_{i-1} + E_i + A(E_i - E_{i-1}) \\ X_{i+1} &= X_i + KF_i \end{aligned} \tag{32}$$

This filter is the discrete analog of the continuous servo:

$$\begin{aligned} F(S) &= K\frac{1 + A\,\Delta\tau S}{(\Delta\tau)^2 S^2} \\ X(S) &= \left[\frac{F(S)}{(1 + F(S))} Z(S)\right] \end{aligned} \tag{33}$$

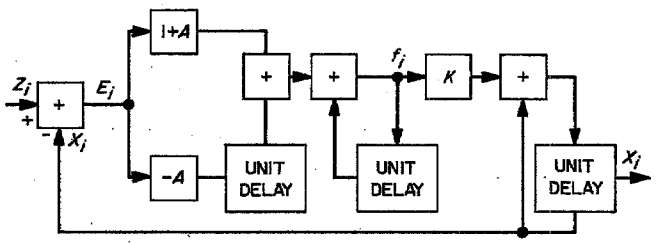


Fig. 35. Second-order sampled data tracking loop

where $\Delta\tau$ is the time-step between the samples of Eq. (32). The behavior of Eq. (33) is well known, and if the response of the filter is slow enough, should closely approximate the behavior of Eq. (32).

The response of Eq. (32) will be investigated by the technique of generating functions. Define

$$G_x(\eta) = \sum_{-\infty}^{\infty} \eta^i X_i \tag{34}$$

and similarly define the generating functions of the other sequences involved in Eq. (32). Applying Eq. (32) to these and manipulating formally, one gets

$$G_x(\eta) = \frac{K\eta(1 + A - A\eta)}{(1-\eta)^2 + K\eta(1 + A - A\eta)} G_Z(\eta)$$

and (35)

$$G_E(\eta) = \frac{(1-\eta)^2}{(1-\eta)^2 + K\eta(1 + A - A\eta)} G_Z(\eta)$$

Applying the final value theorem to the second form shows that

$$\begin{aligned} E_\infty = 0, \quad & \text{if } Z_i = \delta_{i,0} \\ & \text{or if } Z_i = 1,\ i \geqq 0, \quad 0 \text{ before} \\ & \text{or if } Z_i = \alpha i,\ i \geqq 0, \quad 0 \text{ before} \end{aligned} \tag{36}$$

That is, the filter shows the desired zero steady-state error for a pulse, step, or a ramp input. It shows the expected static error for a double ramp input.

Let the pulse response of the digital filter be H_j. Then for any sequence Z_i the sequence X_n is given by

$$X_n = \sum_{j=-\infty}^{n} H_{n-j} Z_j \tag{37}$$

Assume that the Z_j are independent Gaussian random variables with variance V_Z. Then

$$E\{X_n^2\} = E\left\{\left(\sum_{-\infty}^{n} H_{n-j} Z_j\right)\left(\sum_{-\infty}^{n} H_{n-i} Z_i\right)\right\}$$

$$= \sum_{j,i=-\infty}^{n} H_{n-i} H_{n-j} E\{Z_i Z_j\}$$

$$= V_Z \sum_{0}^{\infty} H_i^2$$

$$\triangleq B_H V_Z \tag{38}$$

where B_H is, by definition, the noise bandwidth of the filter H_j. For any fixed value of open-loop gain K, the noise bandwidth B_H is minimized by selecting A to be

$$A_0 = \frac{1}{K^{1/2}} - \frac{1}{2} \tag{39}$$

at which point

$$B_{H0} \approx K \frac{2 + K^{1/2}}{2 - K^{1/2}} \tag{40}$$

Actual choice of the parameters A and K will depend upon the statistics of the (Z_i) and the constraints upon $(X_i - Z_i)$. If the (Z_i) are relatively stable, and initial acquisition performed as an estimation rather than as a tracking process, B_H can be chosen to satisfy jitter requirements at the detector, and A and K chosen from Eqs. (39) and (40). The resultant jitter variance in question is (see Eq. 15):

$$V_X = B_H\left[\frac{1}{8}\left(\frac{N_0}{ST_B}\right)^2 + \frac{5}{32}\left(\frac{N_0}{ST_B}\right)\right] \tag{41}$$

where B_H defines A and K through Eqs. (39) and (40).

f. Loop nonlinearities. Analysis of the bit synchronizer presented so far has treated the tracking loop as if it were a linear sampled servo. There are, however, two nonlinearities which must be accounted for. One of these is shown in Fig. 27 in the decreasing error signal with increasing $|\tau|$ in the region $\frac{1}{4} \leq |\tau| < \frac{1}{2}$. The exact probability distribution of τ may be determined by a technique similar to that used by Viterbi (Ref. 7) for a continuous servo with generalized restoring force. Such refinement is unnecessary, however, as one of the requirements upon the bit synchronizer is that it contribute negligible degradation to the signal. One of the consequent necessary conditions is that the probability that τ is in the range $\frac{1}{4} \leq |\tau| < \frac{1}{2}$ must be virtually zero. Since the loop error signal is linear in τ for $|\tau| < \frac{1}{4}$, the linear servo approximations that have been used must be valid for all situations of interest.

The second nonlinearity does not seem to be so easily dismissible. The nonlinearity in this case is the quantization of bit time—the controlled variable—in the timing generator or NCO. This quantization affects the bit-timing subsystem at two levels:

(1) Bit-time and bit-time-rate offsets due to this discretinization will directly affect bit-error rate.

(2) Quantization of the time variable in the bit-tracking-servo will introduce a "dead zone" and may degrade its performance significantly. These two problems will be treated separately in the following.

Loss due to quantization. Assume that an estimate of bit timing exists separate from the NCO which is exact in rate and phase. Assume further that the NCO is forced to mark the bit time as its allowed state nearest to this correct timing estimate. Any losses (in SNR) arising in this configuration are due directly to the time discretinization, and to no other cause. In the absence of noise, a computer-controlled delay-locked loop in which fine time resolution is maintained in software and a coarser resolution in hardware will closely approximate this operation.

Consider the detection of bit B_1 shown in Fig. 36. The start of the integral defining $\hat{B}_1$ is delayed by τ_p, a phase offset. The end of this integral is delayed by $\tau_p + \tau_R$, where τ_R is bit-duration (rate) error; τ_p and τ_R are measured in fractions of a bit duration. The effective SNR on $\hat{B}_1$ is given by

$$SNR_E = \frac{ST_B}{N_0} \frac{(1 - |\tau_p| - |\tau_p + \tau_R|)^2}{1 + \tau_R} \tag{42}$$

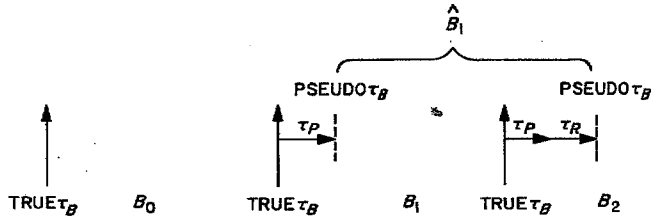


Fig. 36. Detection of a bit stream with improper time references

if the offsets cross a transition, or by

$$SNR_E = \frac{ST_B}{N_0}(1 + \tau_E) \tag{43}$$

if the offset crosses a nontransition. The parameter ST_B/N_0 is the bit energy to noise spectral density ratio.

If the allowed states of the NCO clock times are exactly δ_τ apart, the noiseless selection system will maintain $|\tau_p| \leq \delta_\tau/2$, $|\tau_E| \leq \delta_\tau$; τ_p and τ_E take a sequence of values which is completely determined by δ_τ. An upper bound on the SNR loss is determined by setting τ_p and τ_E at their bounds, i.e.,

$$SNR_E \geq \frac{ST_B}{N_0}\frac{(1 - 2\delta_\tau)^2}{1 + \delta_\tau} \tag{44}$$

This is shown as the upper bound on Fig. 37. For small δ_τ, the expected loss may be approximated by determining the expected value of the SNR_E under the assumption that τ_p and τ_E are independent and uniformly distributed over their allowed range. This is shown as the expected value line on Fig. 37.

It is apparent from Fig. 37 that a δ_τ on the order of 10^{-2} to 10^{-3} will provide the required resolution at the detector.

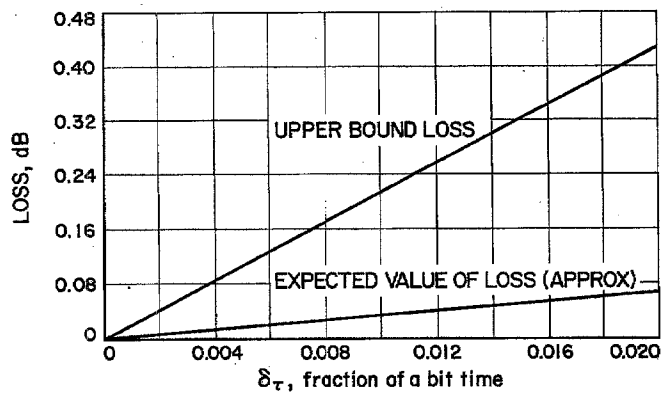


Fig. 37. Loss in signal power attributable solely to discretinization of the time estimate

g. Quantization in the bit-tracking system. A discrete servo-system with quantizer is shown in Fig. 38. We wish to determine here for which values of δ_τ the quantizer may be neglected. In the absence of noise, a dead zone of width δ_τ/K exists which can significantly degrade the system's ability to follow variations on the input signal. The noise, however, will act as a "dither" signal and smooth out the quantizer steps.

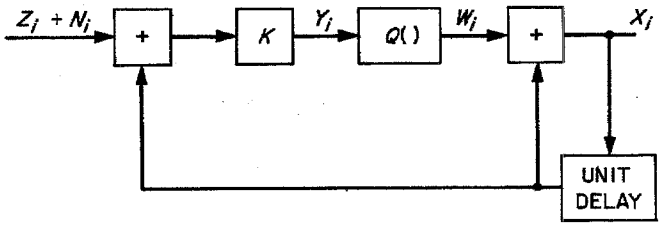


Fig. 38. Discrete servo with quantization:

$$\mathbf{Q(x) = \delta_\tau \left[\!\left[\tfrac{1}{2} + \frac{x}{\delta_\tau} \right]\!\right]}$$

Let the input x to the quantizer $Q(x)$ be a Gaussian random variable with mean μ and variance σ^2. The output variable q is defined by

$$q = Q(x) = \left[\!\left[x + \frac{1}{2} \right]\!\right] \tag{45}$$

where the variables q and x are both normalized with respect to the time step δ_τ.

The expected value of q is

$$E\{q\} = \int_{-\infty}^{\infty} \left[\!\left[x + \frac{1}{2} \right]\!\right] N_{\mu,\sigma^2}(x)\, dx \tag{46}$$

where $N_{\mu,\sigma^2}(x)$ is the normal density function for mean μ, and the variance σ^2. The derivative of $E\{q\}$ with respect to μ is

$$\begin{aligned}
\frac{d}{d\mu}E\{q\} &= \int_{-\infty}^{\infty} \left[\!\left[x + \frac{1}{2} \right]\!\right] \frac{\partial}{\partial \mu} N_{\mu,\sigma^2}(x)\, dx \\
&= -\int_{-\infty}^{\infty} \left[\!\left[x + \frac{1}{2} \right]\!\right] \frac{\partial}{\partial x} N_{\mu,\sigma^2}(x)\, dx \\
&= -\int_{-\infty}^{\infty} \left[\!\left[x + \frac{1}{2} \right]\!\right] d\{N_{\mu,\sigma^2}(x)\} \\
&= \int_{-\infty}^{\infty} N_{\mu,\sigma^2}(x)\, d\left\{\left[\!\left[x + \frac{1}{2} \right]\!\right]\right\} \\
&= \sum_N N_{\mu,\sigma^2}\left(N - \frac{1}{2}\right)
\end{aligned} \tag{47}$$

This series converges rapidly to a function of μ and σ^2 which is periodic in μ with period 1, and symmetric about $\mu = 0$. Figure 39 shows this function for $\mu\varepsilon(0, \frac{1}{2})$ and several values σ. For $\sigma \geq \frac{1}{2}$, the function is 1, and the expected value of q is equal to μ. Applying this to the servo

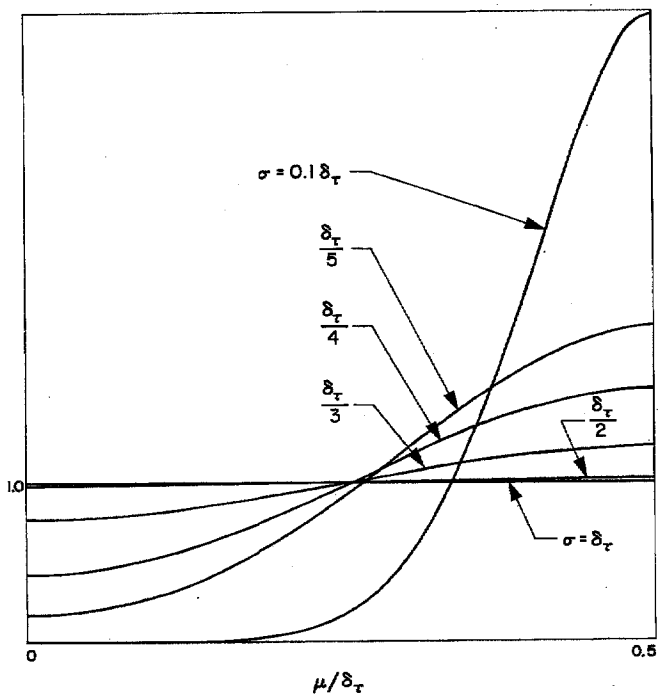


Fig. 39. Derivative of quantizer output with respect to mean of input

of Fig. 38:

$$\text{If } V\{Y_i\} \geqq \left(\frac{\delta_\tau}{2}\right)^2$$

$$\text{Then } E\{W_i\} = E\{Y_i\} \tag{48}$$

Furthermore, if this condition holds for all Y_i, the expected value of X_i is equal to the expected value of the output sequence for an unquantized system. The effect of dead zone may be neglected if Eq. (48) holds.

The system of Fig. 38 may always be represented in the form of Fig. 40. In general, however, the nq_i are functions of the W_i. The condition in Eq. (48) guarantees that

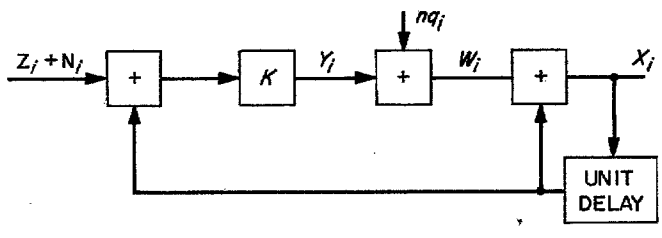


Fig. 40. Discrete servo with quantization noise $nq \in (-\delta_\tau/2, +\delta_\tau/2)$

$E\{nq_i\} = 0$ independent of $E\{Y_i\}$. The effect of the nq_i may thus be approximated by assuming that they are independent of the W_i and distributed uniformly in $[-\delta_\tau/2, \delta_\tau/2]$. Under this assumption

$$V\{X_i\} = \frac{K}{2(1-K)}\left\{V\{n_i\} + \frac{1}{3}\left(\frac{\delta_\tau}{2K}\right)^2\right\} \tag{49}$$

where the X_i follow a quantized distribution with Gaussian envelope. For any fixed value of SNR, Eq. (48) sets a minimal value of K for which Eq. (49) represents a valid model of the quantized system, i.e.,

$$K_{\min} = \frac{\delta_\tau 2\dfrac{ST_B}{N_0}}{\left(2 + 3\dfrac{ST_B}{N_0}\right)^{1/2}} \tag{50}$$

Without quantization, loop gain would be selected on the basis of the jitter statistics of the received bit stream. Since $K_{\min}$ is monotonically increasing in ST_B/N_0, Eq. (50) is most likely to constrain this normal selection process for strong signals. At $ST_B/N_0 = +12$ dB, $K_{\min} = 4.5\delta_\tau$. For $\delta_\tau \approx 10^{-3}$, this constraint $K \geqq 4.5 \times 10^{-3}$ which is probably below the level which the tracking requirements would set.

Using $K = K_{\min}$ in the tracking loop produces

$$V\{X_i\} = \frac{\delta_\tau}{\left(2 + 3\dfrac{ST_B}{N_0}\right)^{1/2} - 2\,\delta_\tau \dfrac{ST_B}{N_0}}\left(\frac{7}{32} + \frac{N_0}{6 \cdot ST_B}\right) \tag{51}$$

which represents the minimum attainable jitter variance. For $ST_B/N_0 = 0$ dB and $\delta_\tau = 10^{-3}$, $V\{X_i\} \approx 1.75 \times 10^{-4}$, which represents an expected loss of $\sim$0.1 dB if the X_i are assumed Gaussian. Equation (51) is plotted as Fig. 41, for various values of δ_τ.

The results of the time discretinization analysis are essentially unchanged if the same arguments are applied to the second-order loop. Refer to Eq. (32) and assume that F_i and X_i are quantized, the other terms are not. Then the variance at the input to the quantizer is

$$V\{q_i\} = K^2(1 + 2A + 2A^2)V_Z$$

$$\approx 2B_{H_0}^2 V_Z \qquad \text{if } A = A_0 \tag{52}$$

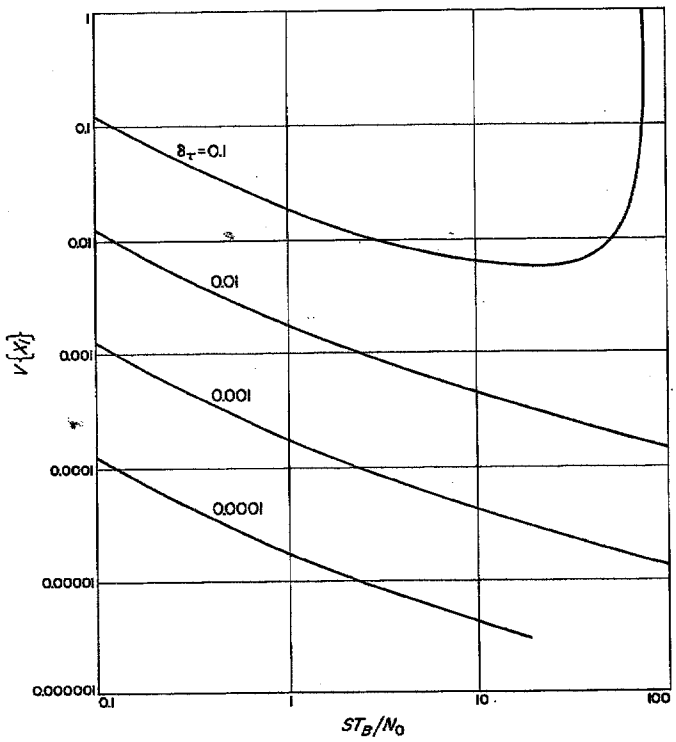


Fig. 41. Irreducible jitter variance versus SNR

Rather than defining a $K_{\min}$, Eq. (48) defines a $B_{H,\min}$ using Eq. (52). The results of Eq. (51) are multiplied by a $(2)^{1/2}$ factor in this process.

The digital timing generator being developed for the MMTS has a resolution of 1 μs. The highest bit rate committed is on the order of 500 bits/s making the largest $\delta_T = 5 \times 10^{-4}$. The conclusion reached is that which could probably have been assumed: that the quantization of bit-timing in the NCO will have negligible effect upon the bit-timing subsystem under current bit-rate constraints.

D. System Verification and Testing, *N. A. Burow, L. Couvillon, and A. Vaisnys*

1. Goals

This part of the MMTS project accomplishes the initial integration and the detailed performance testing of a prototype MMT system. The goals are to prove the system concepts and to verify the results of system analysis. While a prototype MMTS was being built, a system model was used to make some required preliminary measurements, the results of which will be described below. Further experiments will be performed with the prototype system now under construction. It is anticipated that this work will produce the final system parameters and specify the system performance for missions using the MMTS.

2. Approach

Shortly after the MMTS concept was generated, work began on the construction of a model of the system to demonstrate its operation and investigate the practical problems of building such a system. A Scientific Data Systems (SDS) model 920 computer was available, but the RF hardware called for in the early conceptual designs was not. It was therefore necessary to model the system at audio-frequencies; i.e., the 10-MHz bandpass filters were simulated by 100-kHz filters having the same bandwidth. The resulting assembly, which will hereafter be called the baseband breadboard (BBB), very closely duplicates the functions of the actual system design except that the input signal is the subcarrier(s) plus low-passed noise, instead of a phase-modulated intermediate carrier plus band-passed noise. In a sense, the 10-MHz IF has been replaced in the BBB by zero frequency.

Figure 42 is a diagram of the BBB. It shows the subcarrier and data source which generates square-wave subcarriers modulated (phase-shift keyed) by data bit streams, which can be alternate *one-zero*, all *ones*, or long pseudonoise (PN) code sequences. As shown, the bit timing clock may be coherent or noncoherent with the subcarrier clock. The subcarrier(s) thus generated is (are) linearly added to noise in a signal/noise mixer and presented to the BBB demodulator.

The remainder of Fig. 42 will be recognized as very similar to the system block diagram previously explained (Sect. B). The input signal (subcarrier plus noise) is impressed on a 100-kHz IF in the first multiplier[2]. The resulting signal is then fed, in parallel, to two multipliers. In one it is multiplied by a square wave subcarrier reference and in the other by a 90-deg shift of the reference. The 0- and 90-deg reference multiplied signals are band-pass filtered at 100 kHz, one is low-pass filtered and limited, and the two are multiplied together to generate a phase-error voltage which is filtered and controls a VCO. Such a system is recognized to be a form of a Costas phase-lock loop.

[2]The word "multiplier" is used loosely here. In the mechanization, the multipliers are actually choppers.

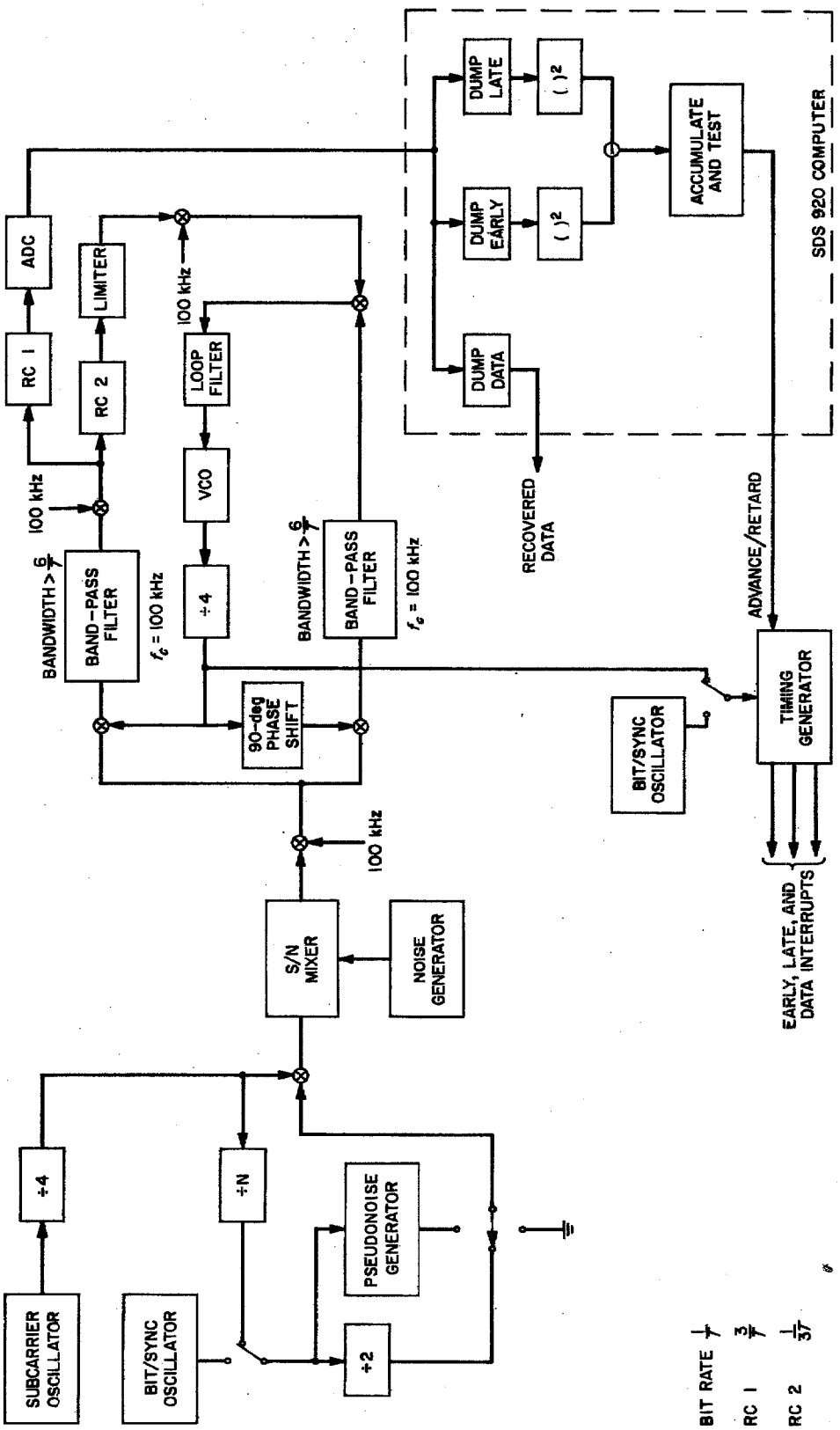


Fig. 42. BBB system diagram

The BBB was built up using Computer Control Co. (3C) digital circuits and operational amplifiers. The choppers are basically operational amplifiers operating in the differential mode. The choppers were designed to operate over a range of 20 mV to 5 V (48 dB). This dynamic range allows operation down to $ST/N_0 = 0$ dB at 6¼ bits/s with a 20-mV signal in a 40-kHz bandwidth, accommodating $\pm 3\ \sigma$ noise peaks linearly. The band-pass filters are of the Q multiplier type with a bandwidth tunable between 1200 and 200 Hz.

Initially, problems were encountered in interfacing the A/DC with the computer, and in the stability of some components, such as the VCO. For example, with the first VCO used, the best performance was obtained with a 2-Hz loop bandwidth. A newer model VCO allowed going to 1-Hz loop bandwidth, and only by using a HP 5100A frequency synthesizer as a VCO was it possible to go to loop bandwidths below 1 Hz and realize any improvement.

As shown in Fig. 42, data demodulated from the subcarrier by the Costas loop is low-pass filtered and digitized. The A/DC enters data to the SDS 920 computer, in which bit synchronization operations are carried out. The algorithm used in the BBB is the same as previously described (Sect. C-4); early and late samples of data are squared, subtracted, and their difference is used to generate a timing error signal. The timing generator circuitry for the BBB was built from 3C logic.

The computer programs for the BBB were written to accomplish only the required control and instrumentation functions for the equipment on hand; no consideration was given to other operations (e.g., decommutation) necessary in the real world or to integration of the software with other TCP functions. The software is organized as several subroutines, executed under interrupt control. Figure 43 is a flow diagram for the BBB bit synchronization program. It may be seen from Fig. 43 that the computer waits for a new interrupt after it has finished an operation requested by a prior interrupt. When a timing error computation has been made, the correction is outputted (POTted) immediately.

For instrumentation purposes, several additional routines have been added to the main program to allow examination of the system at various points, somewhat increasing the required running time. Four additional routines are: (1) computation of the normalized signal-to-noise ratio averaged over 1000 data bits, (2) printout on the line printer of both the corrected and uncorrected digitized data from the two integrators, (3) outputting of the bit timing error values to a digital-to-analog converter to generate the open-loop bit sync error curves for observation, and (4) writing the corrected value of data taken at bit sync time on magnetic tape.

Considerable effort has gone into the design and construction of test instrumentation for the BBB. The test setup has been designed so that it may be used with the prototype system with minimal changes. Some of the system parameters which are accurately measurable with the test setup are bit-error rate, bit clock jitter, subcarrier jitter, bit acquisition time, and effective (internal) SNR.

The instrumentation used in evaluating the system is illustrated in Fig. 44. Bit-error rate tests are handled as follows:

As the data bits are recovered by the computer, they are outputted to a storage flip-flop. A bit-error rate monitor is used to compare the recovered bits with the corresponding bits from the modulator and to count the number of bits transmitted. It stops after a predetermined number of total bits and displays an error count.

Another measurement that is valuable in determining system performance is that of the jitter in the subcarrier loop. Both the subcarrier from the modulator and the recovered subcarrier are fed to a time interval counter which measures the time interval between their corresponding edges. This information is sampled and stored on tape for later analysis.

3. Baseband Breadboard Test Results

Initial runs on the BBB were made at a bit rate of 200 bits/s in order to allow debugging of the system with convenient signal levels and test times. Performance at this bit rate was found to be substantially in accordance with theory. Figure 45 is a plot of bit-error rate versus ST/N_0, the ratio of energy per bit to noise spectral density. The experimental points are seen to be within 0.3 dB of theory; the instrumentation error is estimated at less than ± 0.2 dB at each individual point.

Also measured were the open-loop error curves for the subcarrier and bit-sync loops, Figs. 46 and 47, respectively. Figure 46 is seen to be a sawtooth wave as theoretically predicted; Fig. 47 is a sampled triangular wave, as it should be. These figures are for the case of no noise.

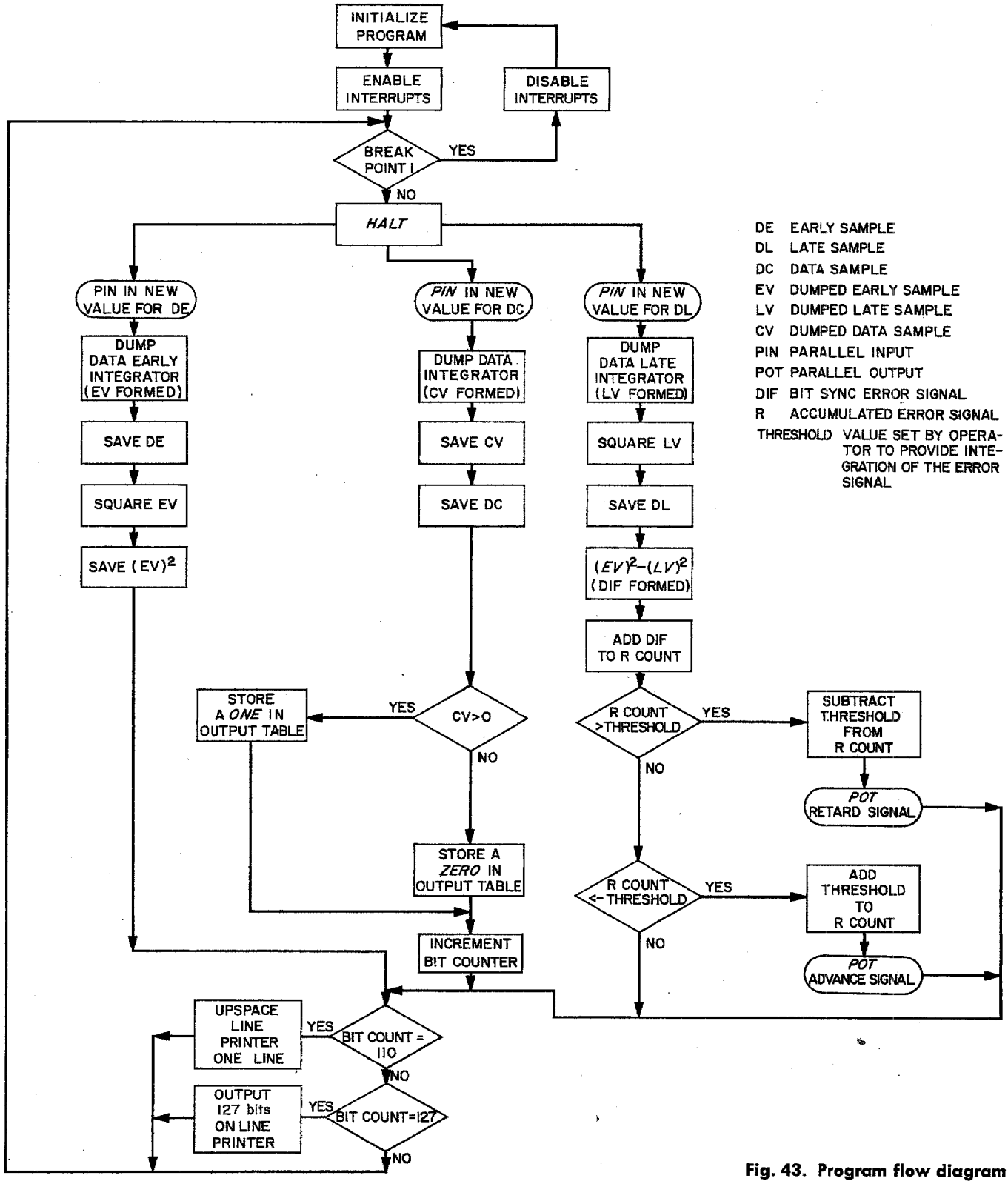


Fig. 43. Program flow diagram

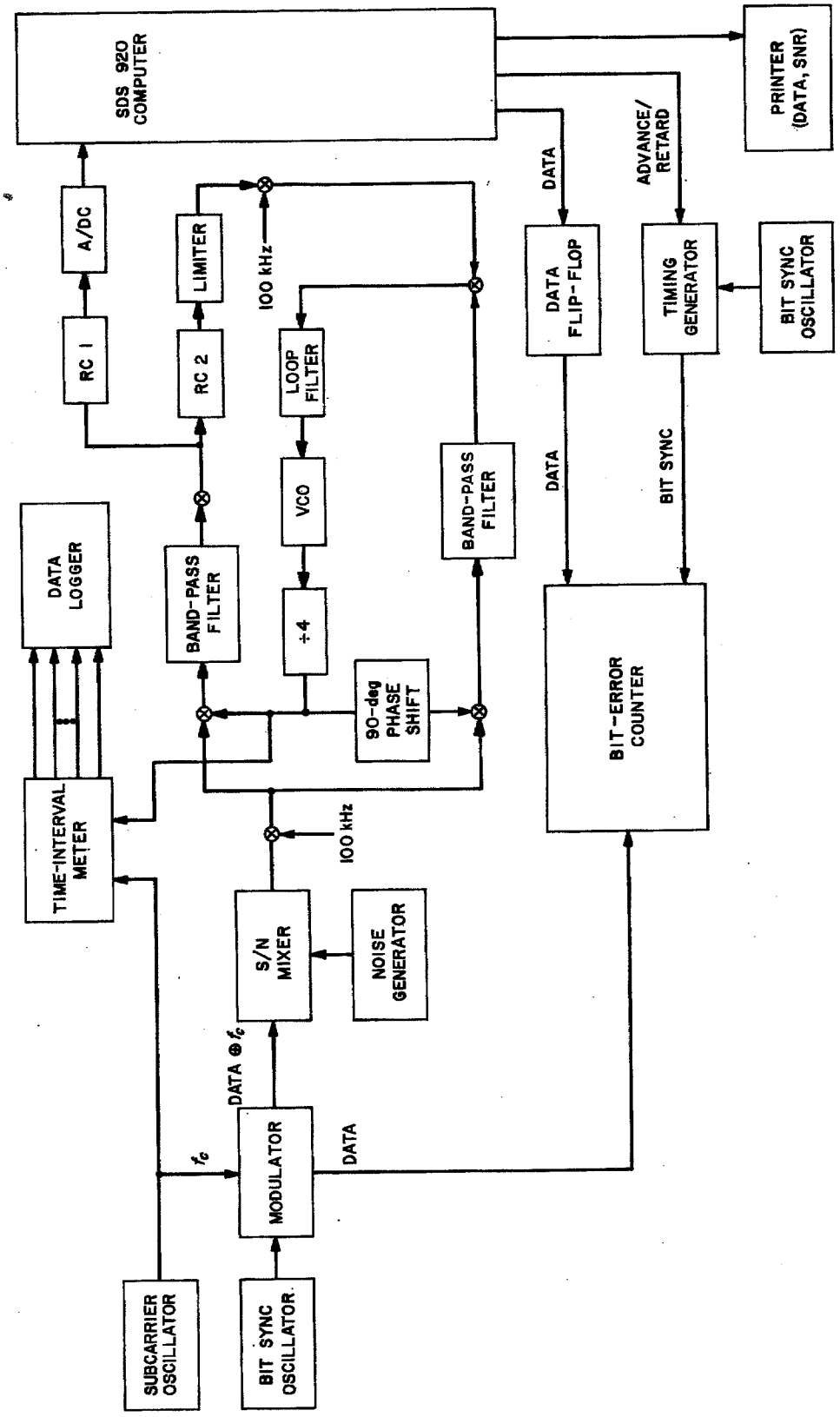


Fig. 44. BBB system test setup

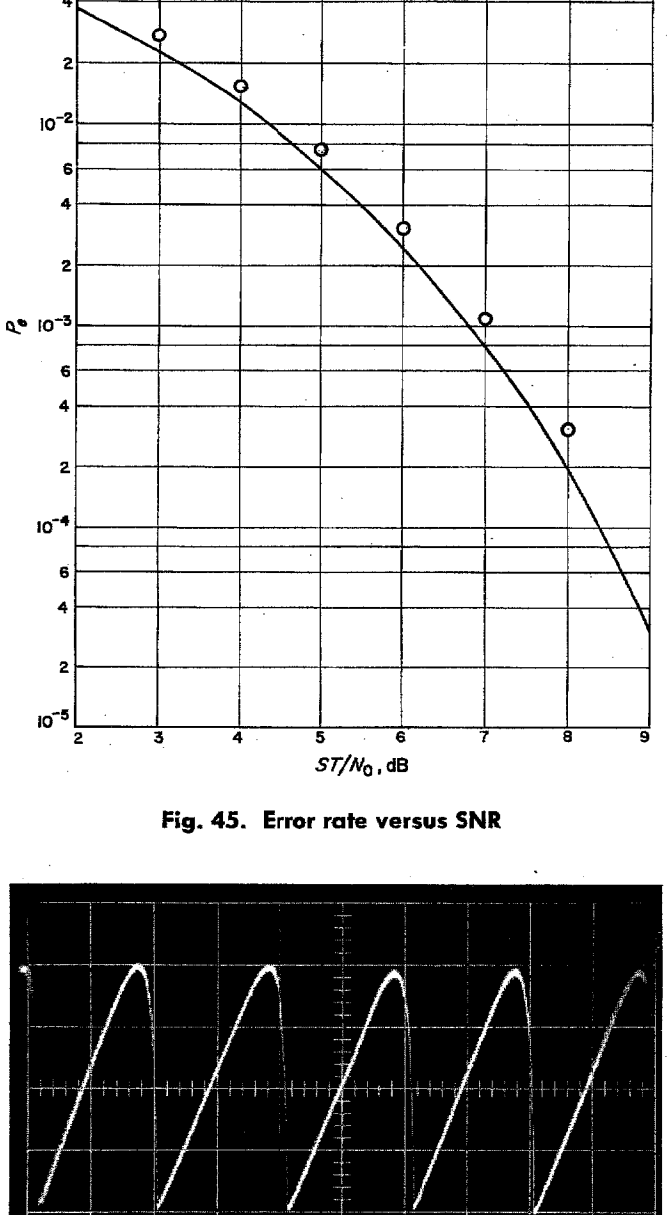


Fig. 45. Error rate versus SNR

Fig. 46. Subcarrier S-curve

Results of error rate tests at lower bit rates were more pessimistic. Several runs have been made at 6¼ bits/s, but the results are not yet conclusive. At 6¼ bits/s, using a 1-Hz subcarrier loop bandwidth, it was found that the degradation due to jitter was on the order of 3 dB. It was

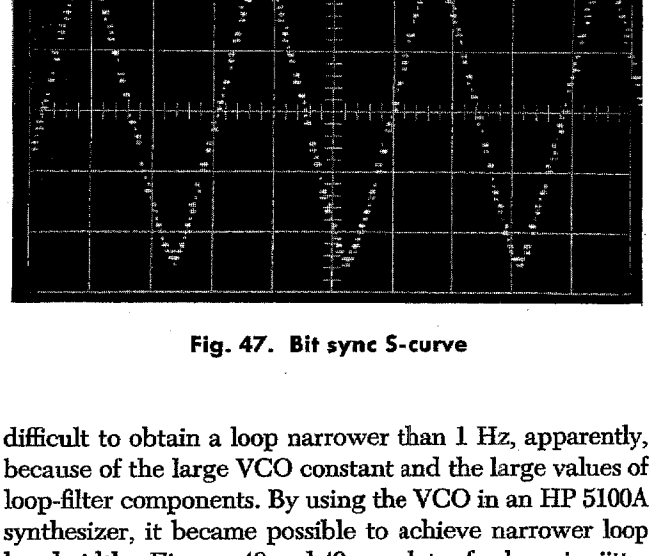


Fig. 47. Bit sync S-curve

difficult to obtain a loop narrower than 1 Hz, apparently, because of the large VCO constant and the large values of loop-filter components. By using the VCO in an HP 5100A synthesizer, it became possible to achieve narrower loop bandwidths. Figures 48 and 49 are plots of subcarrier jitter with loop bandwidths of 1 and ¼ Hz, respectively. Note that there is a substantial dependence of the jitter upon the presence of data modulation.

It is planned, as far as time allows, to further investigate the performance of the loop at low bit rates and to make a trade-off between loop bandwidth, performance degradation, and acquisition time.

4. Net System Verification Plans

A functional description of the net system was given in a previous section of this report. The net system prototype soon to be assembled in the lab is intended to be functionally identical to the systems that will eventually go to the DSN stations. Thus, it is intended to continually update it as design changes or improvements are made.

The test instrumentation to be used in evaluating the prototype will be substantially the same as that used with the breadboard system. A comprehensive test plan is being generated with inputs from each of the groups of the MMT project. The checkout of the prototype system will include, but will not be limited to, the following tests:

(1) The determination of usable and forbidden subcarrier frequencies in the range of 20 Hz to 80 kHz.

(2) Bit-error tests at selected bit rates in the range of 1 to 512 bits/s under various signal-to-noise conditions.

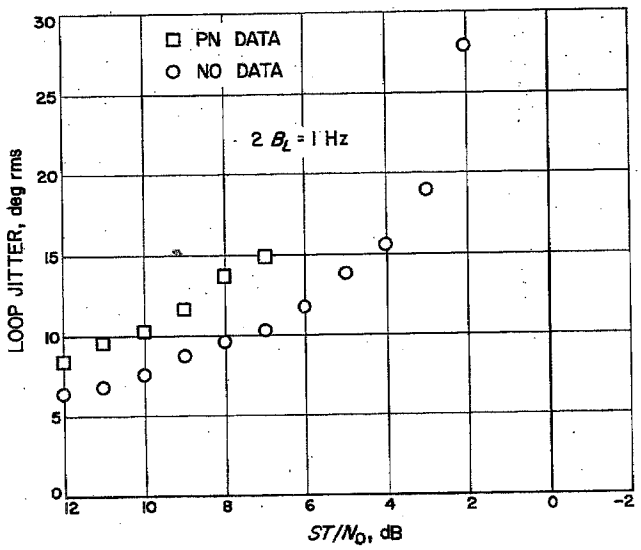


Fig. 48. Subcarrier jitter with 1-Hz loop bandwidth

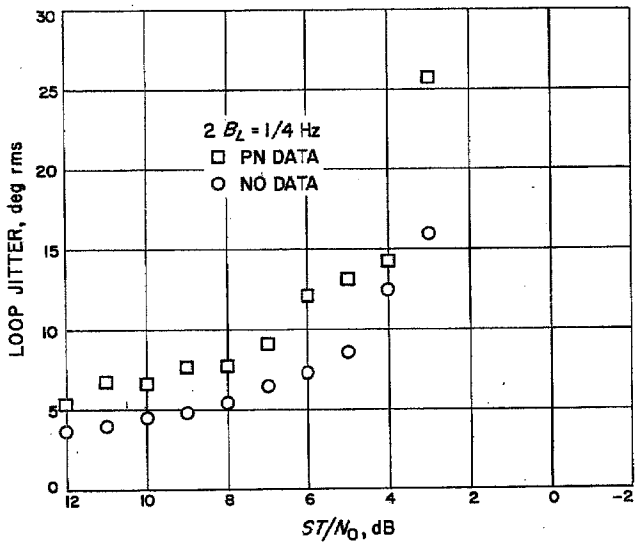


Fig. 49. Subcarrier jitter with ¼-Hz loop bandwidth

(3) Bit-error rate performance as subcarrier tracking loop bandwidth (2 B_{Lo}) varies.

(4) Subcarrier acquisition time as a function of ST/N_0, frequency off-set, and 2 B_{Lo}.

(5) Acquisition properties of the bit-sync loop.

(6) Investigation of performance degradations as they are found.

(7) Evaluation of performance in the magnetic tape playback (system backup) modes of operation.

E. Equipment Description, *J. W. Layland, R. G. Petrie, J. E. Stelzried, and J. K. Woo*

1. Subcarrier demodulator assembly, *J. E. Stelzried*

a. Electrical characteristics. The basic design philosophy incorporated into the subcarrier demodulator assembly (SDA) was compatibility and maximum equipment interchangeability with the existing receiver-exciter (R-E) subsystem and other DSN equipment.

b. Performance characteristics. This equipment is designed to demodulate data that is biphase-modulated on a subcarrier which is phase-modulated on a 10-MHz IF signal derived from the R-E subsystem. Pertinent parameters of this signal are as follows:

Subcarrier power	−70 dBmW ±15 dB
Subcarrier frequency	20 kHz to 1 MHz
Subcarrier doppler	$1 \times 10^{-5} \times F_{sc}$
Subcarrier to noise ratio	−77 dB maximum (bandwidth, 2 MHz at 1 dB)
Data rates	8 to 512 bits/s

A hardware block diagram of the SDA is shown in Fig. 50. This equipment contains a considerable amount of hardware applicable to future expansion capabilities for both high and low data-rate options, as described in more detail later in this report. In order to demodulate the data under all variable conditions of data rates, doppler rates, subcarrier frequencies, and output SNRs, system-selectable parameters were provided for the prototype SDA to evaluate for use in the DSIF. They are listed in Tables 1 to 6.

Table 1. Variable loop bandwidth (2 B_{Lo}) selector

Selector position	Loop bandwidth 2 B_{Lo}, Hz	Nominal data rate, bits/s
1	0.010	1.0–2.2
2	0.022	2.2–4.7
3	0.047	4.7–10
4	0.10	10–22
5	0.22	22–47
6	0.47	47–100
7	1.00	100–220
8	2.20	220–470
9	4.70	470–1000
10	10.0	1000–2200
11	22.0	2200–4700
12	47.0	4700–10K
13	100.0	10K–22K
14	220.0	22K–47K
15	470.0	47K–100K

Variable loop bandwidth selector. The loop bandwidths and nominal data rates are given in Table 1.

This selector also controls the tracking or acquisition tuning range capabilities of the loop as defined in Table 2

Table 2. Tracking or acquisition tuning range capabilities of the loop

Selector position	Acquisition tuning range, Hz
1–3	±2
4–6	±20
7–9	±200
10–12	±2000
13–15	±20,000

Data-rate selector. The data-rate selector provides variable RC integration time constants (T_D) for the prime data outputs, loop reference RC filter time constants (T_S) that precede the data limiter, the lock indicator relay time constant (T_L), and 10-MHz IF filter bandwidths as noted in Tables 3, 4, 5, and 6.

Table 3. Integration time constants for data outputs

Selector position	Time constant T_D, ms
1–3	3300.00
4–6	330.00
7–9	33.00
10–12	3.30
13–15	0.330

Table 4. Loop data filter time constants and lock detector error-channel signal time constants

Selector position	Time constants T_S and T_E, ms	Data rate, Hz
1	220.0	1.0–2.2
2	100.0	2.2–4.7
3	47.0	4.7–10
4	22.0	10–22
5	10.0	22–47
6	4.70	47–100
7	2.20	100–220
8	1.00	220–470
9	0.47	470–1000
10	0.22	1000–2200
11	0.10	2200–4700
12	0.047	4700–10K
13	0.022	10K–22K
14	0.010	22K–47K
15	0.0047	47K–100K

Table 5. Filter time constants of lock indicator relay

Selector position	Time constant T_L, s
1–3	50.000
4–6	5.000
7–9	0.500
10–12	0.500
13–15	0.500

Table 6. 10-MHz IF filter bandwidth

Selector position	IF bandwidth (−1 dB), kHz
1–2	Low data option
3–5	0.50
6–9	10.00
10–12	100.00
13–15	1000.00

c. Block diagram description. A hardware block diagram of the SDA is shown in Fig. 50. The numbered blocks represent individual subassemblies and indicate their specification numbers, while the large blocks represent panel-mounted equipment with small internal blocks representing separate functions inside these panel-mounted units. For discussion purposes, the block diagram may be broken down into the following categories: input distribution, data channel, error channel, lock detector, and reference distribution.

Input distribution. The input signal to the SDA may be selected from one of four sources:

(1) 10-MHz input. This is the normal mode of operation. The 10-MHz signal is supplied from receiver 1 of the R-E subsystem, routed through the 10-MHz baseband relay, level set attenuator, and then distributed to the data and error channels via the 10-MHz IF distribution amplifier subassembly (9465). An auxiliary output of this signal is routed to the interface panel. The level set attenuator is variable in 1-dB increments over a 50-dB range. Its setting is dependent upon the modulation index of the subcarrier onto the carrier (0.1 to 1.27 rad); it also equalizes the various baseband inputs to the equivalent 10-MHz input.

(2) Tape input. This baseband signal is supplied from the recording subsystem as a backup mode of operation. A baseband signal consists of a subcarrier biphase-modulated with data. This signal is routed through the baseband selector relay to the balanced modulator (9577). This unit modulates a 10-MHz reference signal with the baseband signal. The

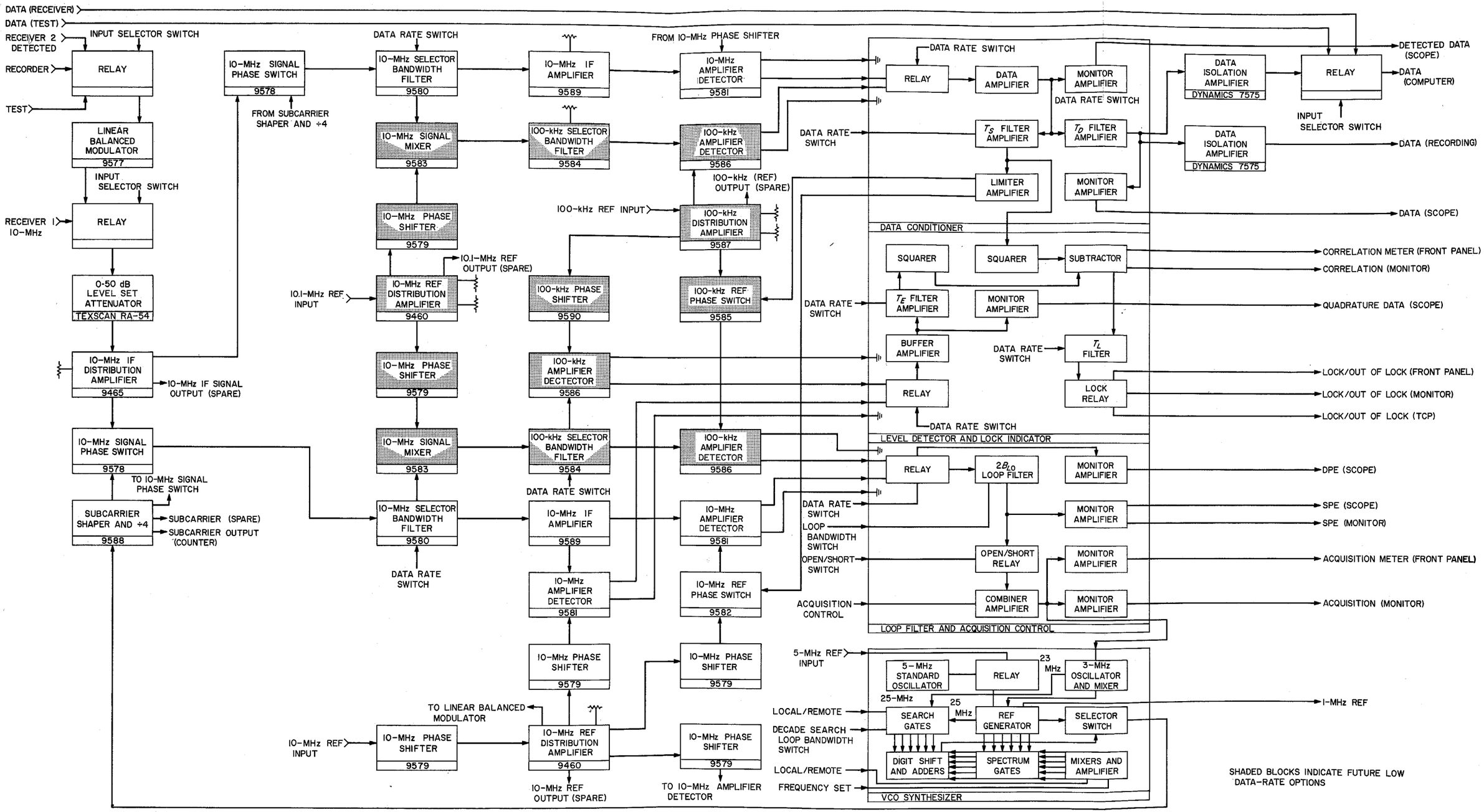


Fig. 50. SDA block diagram

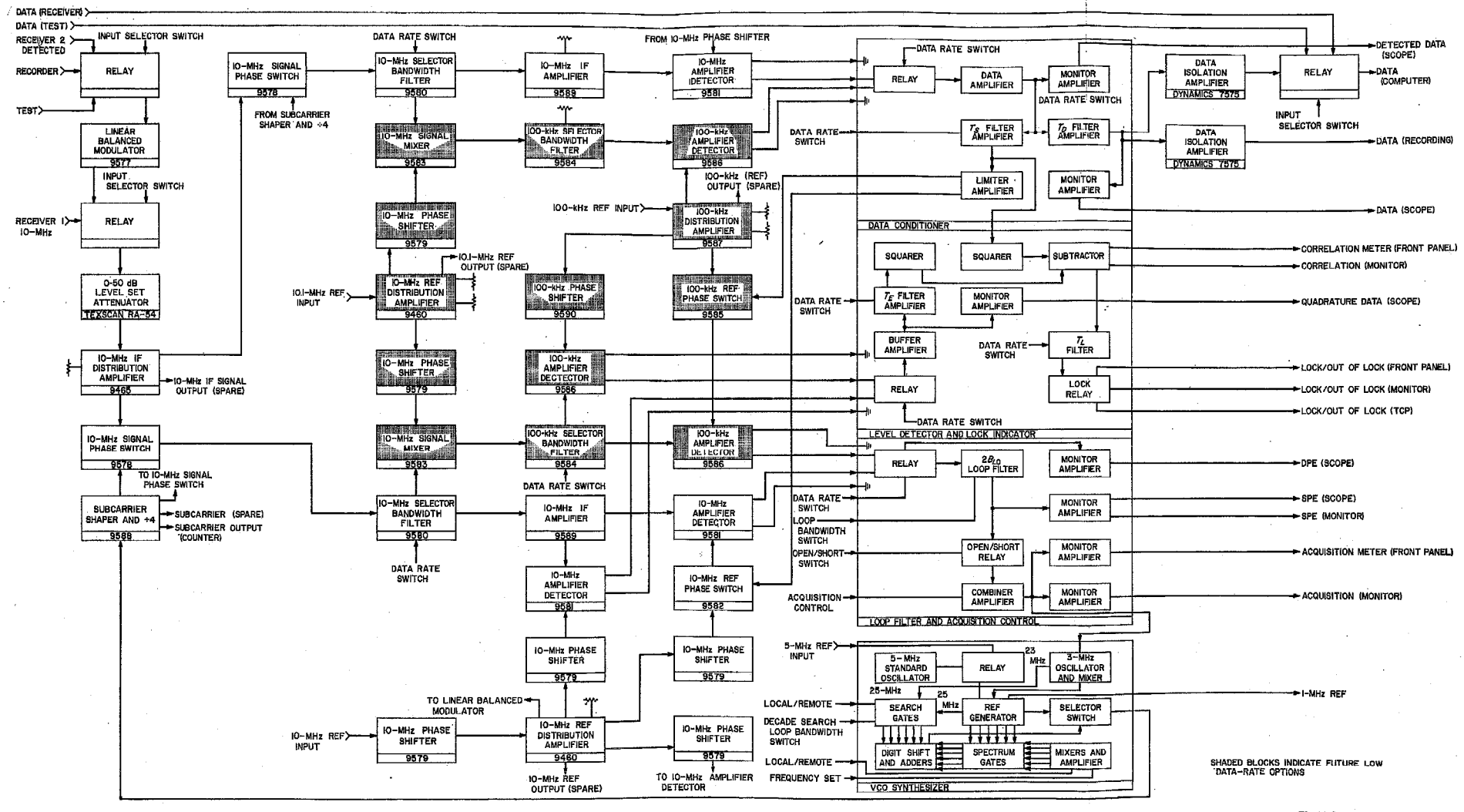


Fig. 50. SDA block diagram

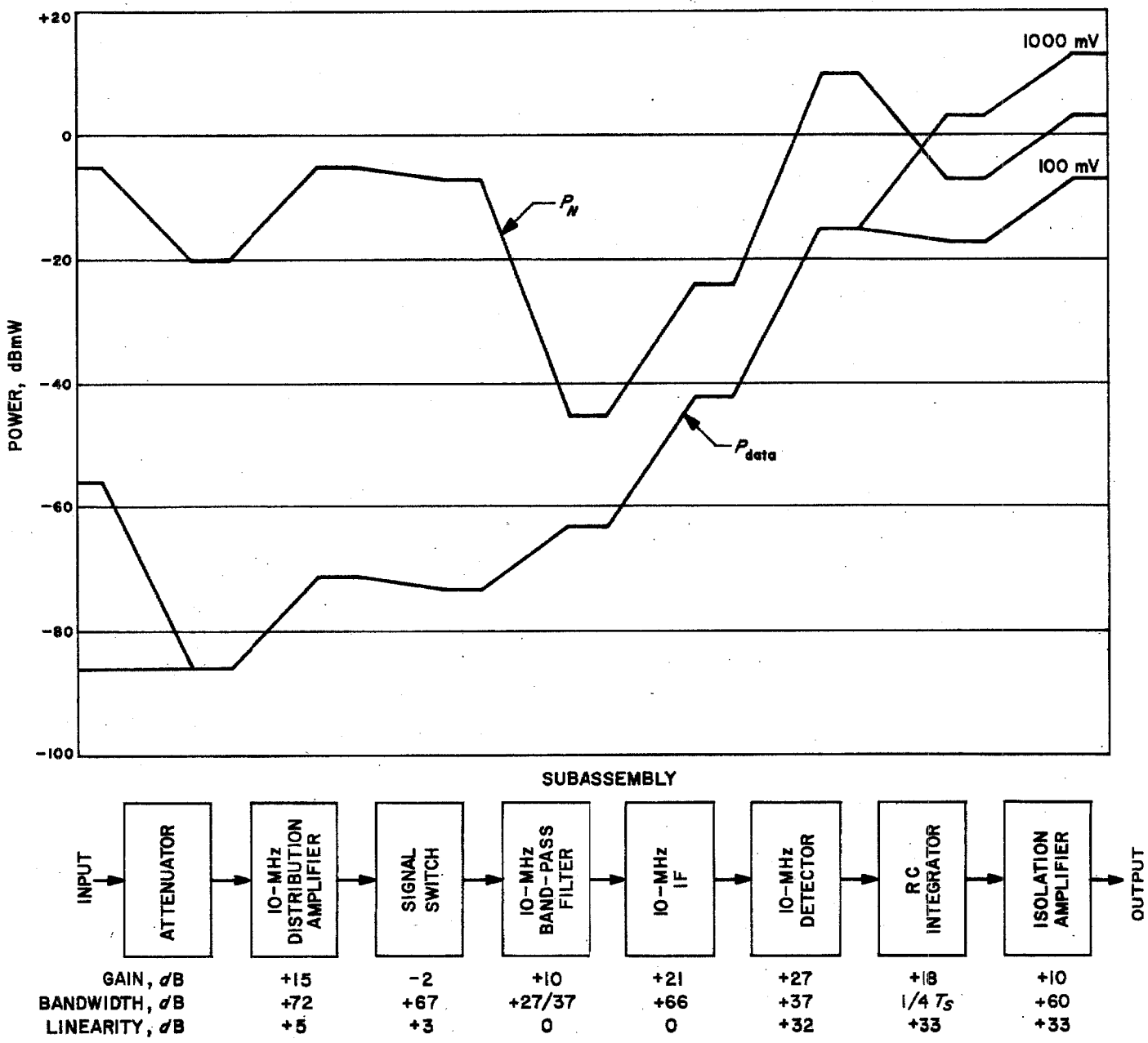


Fig. 51. Power profile curve

This synthesizer is operated at four times the incoming subcarrier frequency. The reason for this is that the synthesizer output must be converted into two signals, separated from each other by 90 deg. This process is accomplished in the subcarrier shaper and ÷4 subassembly. This unit accepts the synthesizer output, converts it to a square wave via a shaping circuit, divides by four in a pair of integrated-circuit flip-flops, and then is fed via isolation stages to the two signal phase switches. The purpose of the ÷4 portion of this circuit is to ensure accuracy of the 90-deg phasing between the two signals and also to maintain good square-wave symmetry in each signal component. This symmetry ensures 10-MHz carrier suppression in the phase switch which is essential in the operation of this loop. If the loop is stressed due to doppler, the suppress carrier signal will tend to become less suppressed, since the quadrature phasing in the signal switch will not be ideal. This will cause a dc output from the amplitude detector of the proper polarity to be injected into the loop filter. This dc will tend to shift the synthesizer frequency so as to cause a reestablishment of the 90-deg phasing of the signal switch.

Lock detector. The lock detector has two signals input. One is derived from the filtered data amplifier as described in Sect. E-1-c. The other is derived from the error channel 10-MHz IF amplifier. This signal is detected in a 10-MHz amplitude detector which has an input phase coherent to the common 10-MHz system reference. This detector output is also filtered by a low-pass RC integrator. The filter time constant is selectable and is controlled by the data-rate selector switch. The filter time constants are the same for both inputs and are as outlined in Sect. E-1-b. These two filtered inputs are then buffered and sent to two identical squaring circuits. The squared outputs are then subtracted in a combining amplifier. This combined output is then monitored on a correlation meter and further filtered in another RC low-pass circuit. The time constants of this filter are also controlled by the data-rate selector switch. The output of this filter is then fed to an in-lock relay driver-amplifier that also has a dc level set control (internal) input. This control is adjusted for optimum threshold lock indication. The relay actuates a front panel lock-indicator light.

Three alternate systems for in-lock indication and acquisition aid are under investigation (if any of them prove superior to this lock indicator, a substitution will be made):

(1) Monitor functions. All front panel controls that are normally operated or indicated are monitored by relay closures or voltages by the station monitor. The only exception to this is the input level set attenuator. This setting is indirectly monitored by the correlation meter voltage. All switch positions are monitored by relay closures except the synthesizer frequencies which must be monitored by a counter via the ÷4 subassembly. All three indications (SPE, acquisition, correlation) are monitored by buffer amplifiers that supply ±5 V maximum to the station monitor.

(2) Remote control capabilities. All normal operator control functions are capable of remote control for future computer programming of this equipment. The only exception to this philosophy is the input level set attenuator. The reason for this is that no commercial equipment is known that will economically supply this function without introducing objectional phase shift into the signal path. A search for a suitable unit will continue.

(3) Limitations. There are several limitations to this system that must be observed. One of these is that subcarrier frequencies that are harmonically related to the 10-MHz carrier signal must not be used. This is because even large ratio subcarrier harmonics of 10 MHz will be amplified by the 10-MHz IF amplifier and will saturate the phase detectors. Another limitation is that care should be used in selecting proper data to subcarrier ratios. The fifth harmonic of data rates should be lower than the subcarrier rates or intermodulation products could cause reduced signal power. If high doppler rates are anticipated, high subcarrier frequencies should be utilized in order to better optimize nominal loop filter bandwidths.

Reference distribution. The reference signals (10, 10.1, and 0.1 MHz) are all derived from the R-E subsystem at a nominal level of +10 dBmW. The 10-MHz signal is the only reference needed under present requirements. The other two are for the future low data-rate options. All distributed signals are also at a nominal +10-dBmW level. The input 10-MHz phase shifter (9579) is for establishing correct phase between the incoming 10-MHz carrier and the baseband reference 10-MHz signal. The three output 10-MHz phase shifters are for establishing correct phasing between the data error and lock detector channels relative to the input 10-MHz carrier.

d. Mechanical characteristics. The basic design philosophy incorporated into the SDA was mechanical compatibility with the existing R-E subsystem in the areas of appearance, operator controls, and packaging techniques.

Front panel description. The overall front panel configuration of the SDA is shown in Fig. 52. The following is a list of the panels shown in this view:

(1) Power panel—includes a running time meter and primary ac power switch.

(2) Isolation amplifiers—includes two data amplifiers and one spare (Dynamics type 7575).

(3) Oscilloscope—Tektronix type 503.

(4) Oscilloscope selector—switch for selecting various monitor displays.

(5) Control panel—includes the following controls and displays:

(a) SPE meter indicator.
(b) Correlation meter indicator.
(c) Acquisition meter indicator.
(d) SDA lock/out-of-lock indicator.
(e) R-E lock/out-of-lock indicator.
(f) Input selector modes—test/receiver 2/tape/10-MHz.
(g) Loop filter selector—short/momentary/normal.
(h) Output selector—test/data/tape.
(i) Level set attenuator—0–50 dB.
(j) Acquisition control potentiometer.
(k) System operation—local/remote.
(l) Data-rate selector—15-position push-indicate switch.
(m) Loop bandwidth (2 B_{Lo}) selector—15-position push-indicate switch.

(6) Synthesizer—Fluke type 314B-7.

(7) Blank panel—may become remotely controllable variable attenuator.

(8) Subassembly drawer 1—input signal units.

(9) Subassembly drawer 2—data channel units.

(10) Subassembly drawer 3—low rate data channel units.

(11) Subassembly drawer 4—error channel units.

(12) Subassembly drawer 5—low rate error channel units.

(13) Subassembly drawer 6—reference distribution units.

(14) and (15) Power supplies – HP type 6255A.

Hardware description. There are normally two subcarrier demodulator assemblies associated with each R-E

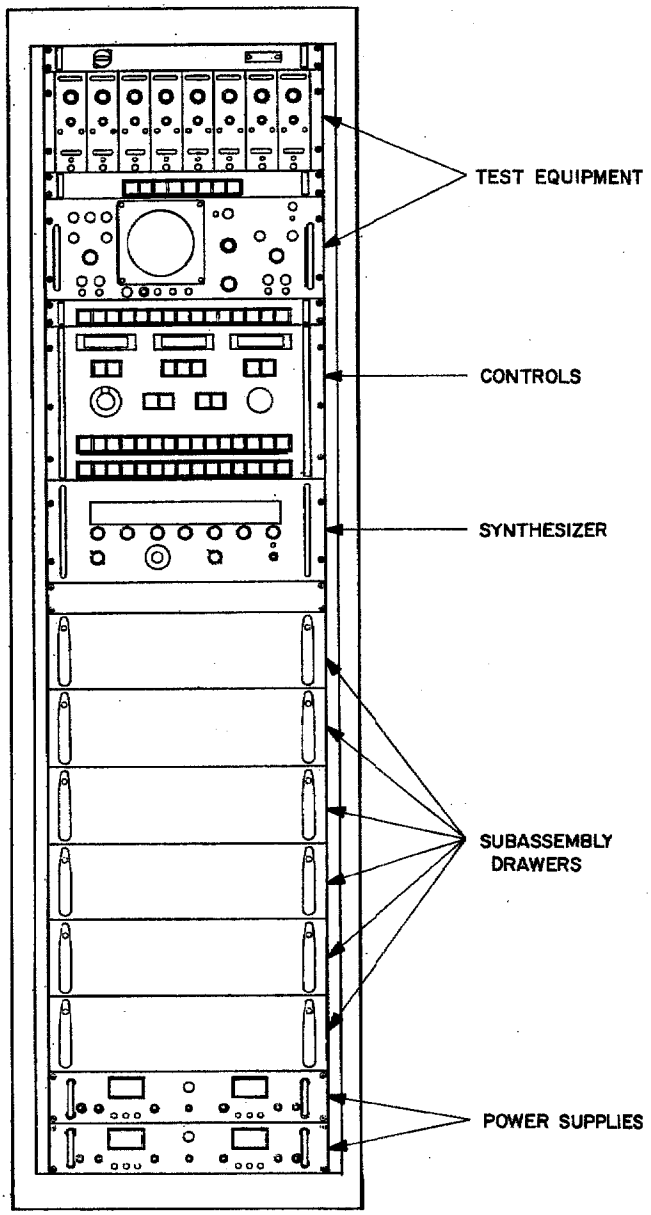


Fig. 52. Front panel configuration of SDA

subsystem. Each is identical and has been designed to be self-contained in the interest of fail-safe operation, except for necessary inputs from other sources. In order to be completely contained in a standard DSIF rack, while providing future low data-rate expansion capabilities, a higher packaging density was found to be necessary than that utilized in the R-E subsystem. One method to be employed is the use of subassembly drawer mounting rather than vertical plate mounting. Careful layout has achieved at least a 40% packaging density capability

increase. Another technique to be employed is packaging the loop filter, data conditioner, and lock detector circuitry in a common drawer, the front panel of which is the operator control panel. This approach will achieve much greater utilization of internal rack space.

e. Expansion capabilities. This equipment has capabilities for future expansion that include both high and low data-rate options.

Low data rate. The definition of low data rates are from 1 to 8 bits/s, biphase-modulated onto existing subcarrier rates.

This option is accomplished by the installation of the shaded subassembly blocks shown on the SDA block diagram (Fig. 50). Operation in this mode is accomplished by signal relays as operated by the existing data-rate selector. It is anticipated that the selectable IF filter bandwidths (as shown in Table 6) will be reassigned to the values shown in Table 7.

Table 7. IF filter bandwidths with low data-rate options

Data rate selector	IF bandwidth (−1 dB), kHz	IF frequency, MHz
1–3	0.10	0.10
4–6	1.00	0.10
7–9	10.00	10.00
10–12	100.00	10.00
13–15	1000.00	10.00

The purpose of these low data-rate subassemblies is that the 100-Hz IF filter shown in Table 7 is beyond the present state of the art at a center frequency of 10 MHz. It is, therefore, necessary to translate the 10-MHz spectrum down to 100 kHz which is accomplished in the 10-MHz signal mixer subassembly (9588).

High data rate. The definition of high data rates are from 512 to 100,000 symbols/s, biphase-modulated onto subcarriers as high as 1 MHz.

This option will be accomplished by the substitution of existing subassemblies with units of wider bandwidths and greater dynamic range. The units that will need substitution, and their parameters, are still under evaluation by the high data-rate project.

f. Engineering evaluation. A preliminary prototype of the SDA has been assembled. It was installed in two low-boy racks for ease of portability (Fig. 53). A typical subassembly drawer is shown in Fig. 54. This drawer is similar to the ones planned for the final version.

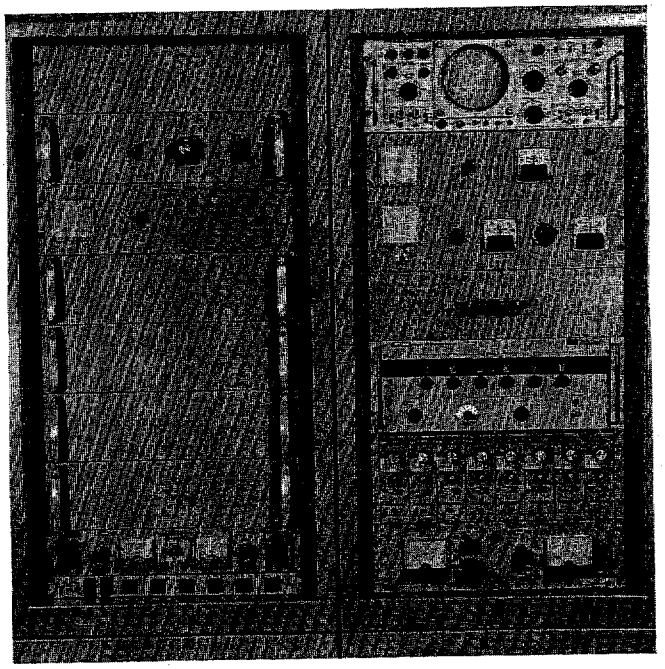


Fig. 53. SDA prototype equipment

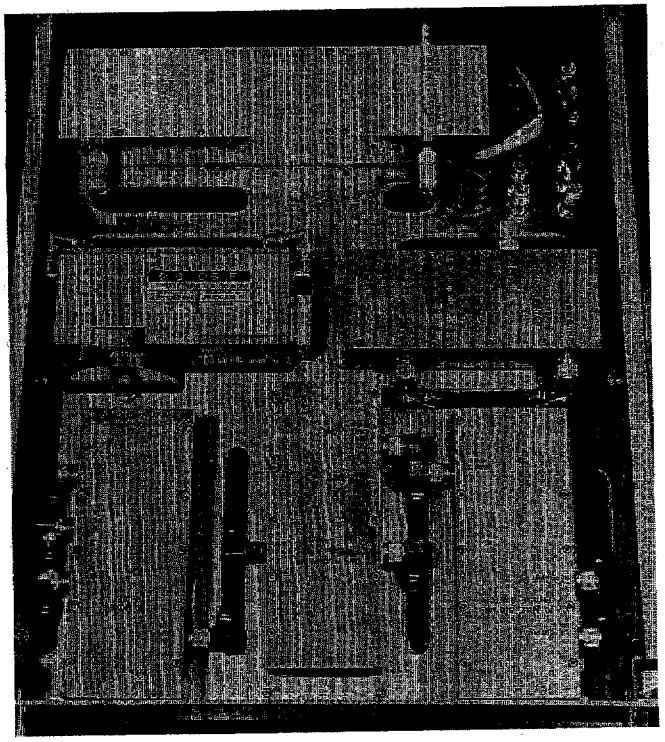


Fig. 54. SDA prototype drawer configuration

This initial assembly is an electrical equivalent of the final design, except no space is provided for the low data-rate option. The unit has been checked out operationally and delivered for system verification testing (see Sect. IV above). Due to time limitations caused by tight scheduling, very little data has been taken on this prototype as of this writing. Capabilities of locking the loop under threshold conditions have been demonstrated with a loop bandwidth of 0.01 Hz.

g. Problem areas. The design process is still continuing on many of the system parameters detailed above. Further system evaluation of several problem areas may cause changes to these parameters. A detailed analysis of these problems is not possible at this time due to lack of sufficient data and definition. The major known problem areas are listed below.

IF bandwidths. Care must be used to select practical bandwidth numbers and sufficient number of filters to protect the dynamic range of the amplitude detectors.

Synthesizer stability. The commercial synthesizer/VCO must be capable of satisfying the stability requirements of low, medium, and high data rates under all conditions of selected subcarrier frequencies, doppler rates, and tape stretch in the spacecraft.

Lock indicator. Threshold resolution of the above detailed indicator may be marginally acceptable. Optional circuits are at present objectionably complex.

2. Computer and Digital Equipment—Telemetry Command Processor, Phase IIC (TCP-IIC),

J. K. Woo and R. G. Petrie

a. Introduction. The TCP-IIC is an expansion of the existing DSIF TCP-II assembly which is described in SPS 37-38, Vol. III, pp. 76, 77. The primary objective of the TCP-IIC is to provide the DSIF station with the capability of converting the undetected data stream from the subcarrier demodulator assembly to a formatted data bit stream for recording and transmission to the SFOF under real-time computer control. In addition to this primary function, the TCP-IIC monitors status of certain receiver assembly and demodulator assembly indicators and converts this station data into the proper format for recording and transmission with the telemetry data.

TCP-IIC will add the following capabilities to the DSIF: (1) determine bit timing and detect bit information from the subcarrier demodulator undetected binary data stream, (2) format the detected bit information for digital recording and transmission to the SFOF, (3) monitor the status of receivers in-lock and demodulators in-lock indications, (4) convert station data, receivers automatic gain control, and static phase error for digital recording and transmission with the telemetry data.

The principal elements of the TCP-IIC assembly are two SDS 920 computers, associated peripheral equipment for input/output, magnetic tape recorder, digital phase shifter for bit-timing control, interface equipment for data transfer and conversion, and communication buffer for direct communication with the SFOF. The TCP-IIC is composed of two independent assemblies, designated as Alpha and Beta, providing a completely redundant data-processing capability. In the event of failure in the primary assembly, the alternate assembly may assume the responsibility of data processing. The switchover from one assembly to the other is rapidly and reliably accomplished through a preprogrammed patch board.

The major equipment elements of TCP-IIC are shown in Fig. 55 and their functional characteristics are described in the following sections:

Transfer rack. The transfer rack is part of the TCD subsystem and its primary functions are to: (1) provide an input interface cable terminus for the subcarrier data streams, receiver AGC and SPE, subcarrier demodulator in-lock, carrier loop in-lock indications and test data, and (2) provide quick-patch capability for switching the set of input data between the Alpha and Beta assemblies. Switching is performed by changing programmable patch boards.

Assembly computer and peripheral equipment. The computer and peripheral equipment in collaboration with the analog-to-digital converter and the digital phase shifter perform the primary functions of data detection and formatting for recording and transmission. The data-detection process consists of bit-time determination and bit-detection operations which are controlled by mission-independent software defined by DSIF and implemented by the project. The formatting of detected bit stream is a function of the mission-dependent software supplied by the project.

The computer is a general-purpose SDS 920 computer with the following characteristic features:

(1) 16,384 words of core memory.

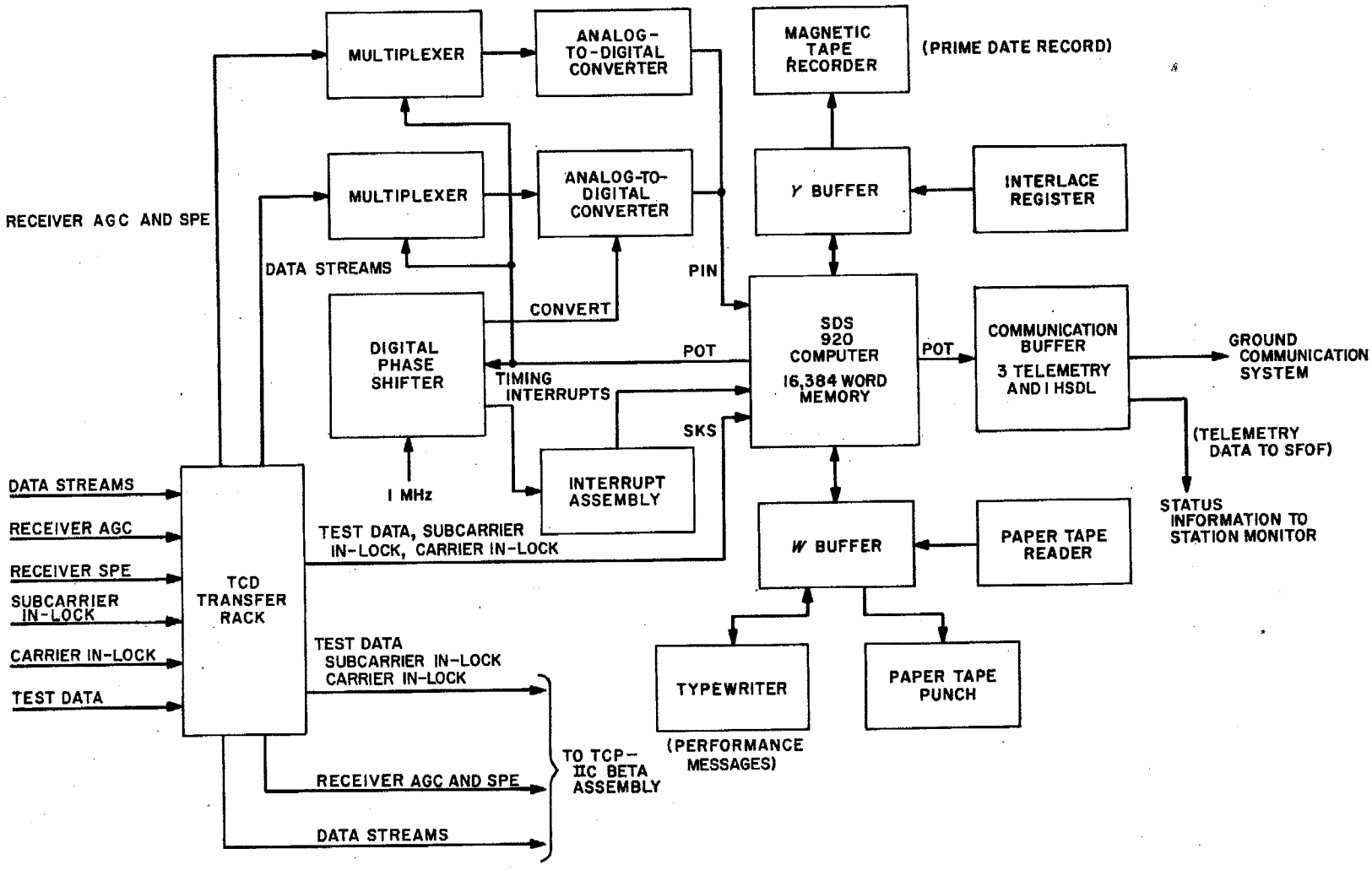


Fig. 55. TCP-IIC Alpha assembly

(2) Word size: 24 bits plus parity check bit.

(3) Arithmetic type: binary, *two's* complement for negative numbers.

(4) 8-μs memory access time.

(5) 16-μs add time (fixed point).

(6) 32-μs multiplication time (fixed point).

W-buffer (Input/Output). A 6-bit character buffer operating with a 24-bit word register provides for communication between computer and paper tape reader, paper tape punch, and typewriter.

Paper Tape Reader. Programming information contained on perforated paper tape is optically scanned at a rate of 300 characters/s and presented to the computer in a character serial format. The paper tape reader operates through the *W* input/output buffer.

Paper Tape Punch. Output data may be perforated on paper tape under computer control at a rate of 60 characters/s and presented by the computer in the character serial format. The paper tape punch operates through the *W* input/output buffer.

Typewriter. Computer-generated performance messages are presented in printed form by the typewriter output at a rate of 10 characters/s. Programming information may be entered into the computer by way of the manual keyboard. The typewriter operates through the *W* input/output buffer.

Priority Interrupt Assembly. Early, late, and bit timing interrupt signals generated by the digital phase shifter interrupt the MMTS computer program and perform specific programmed functions established for each interrupt. An interrupt patch panel is provided to allow for arranging these interrupts into any desired priority.

Y-buffer. The *Y*-buffer is identical to the *W*-buffer, and its function is to provide communication between computer and magnetic tape recorder for the recording of prime telemetry data.

Magnetic Tape Recorder. A magnetic tape recorder provides the capability of recording digital data in an IBM compatible format (binary or binary-coded decimal, 6-bit plus parity) at 200 characters/in. Under computer program control, the prime telemetry data will be recorded at the rate of 15,000 characters/s.

Interlace Register. A 26-bit register operates in conjunction with the *Y*-buffer. The register is divided into two parts, a 12-bit counter that holds the number of words in a data block and a 14-bit address designates the initial memory address into which prime telemetry data are to be obtained. Complete data transfer can be accomplished at rates up to 200,000 characters/s without interfering with other activities of the computer. This facility will permit the computer to operate with simultaneous telemetry-data processing and recording.

Parallel Input/Output. The computer system provides the capabilities of: (1) accepting analog-to-digital converter output data in parallel to the computer, (2) presenting timing and telemetry data in parallel to the digital phase shifter and the communication buffer, respectively. Data transfer is accomplished at rates up to 25,000 words/s with a word length up to 24 bits.

Skip an External Signal (SKS). A computer input signal used to test the status of subcarrier in-lock, carrier in-lock indicators and the data input from the test equipment.

Digital phase shifter.

General. The function of the digital phase shifter/timing generator is to provide the computer program timing signals coherent with the data-bit transition times. In order to establish and maintain coherence, the phase-shifting capability permits adjustment of the timing signals as directed by the program. The timing generator also provides a signal every ¼-bit time ($T_b/4$), since the timing algorithm requires early and late signals in addition to the bit time signal. A block diagram of the phase shifter/timing generator is shown in Fig. 56. Additional functions are detailed in the following description of the theory of operation.

Theory of Operation. The phase shifter is composed primarily of two binary registers, a limit detecting gate, and a transfer logic network. One register, the holding register, contains a number, in effect, equal to the number of microseconds in ¼-bit duration. The other register, the counting register, starts initially with the value contained in the holding resigter, and counts backwards at 1-μs intervals until the register reaches *zero*, when it is again reset to the value contained in the holding register. The transfer logic network is used to set the counting register to the correct initial value and is energized by the limit detecting gate, which senses when the counter has reached its lower limit.

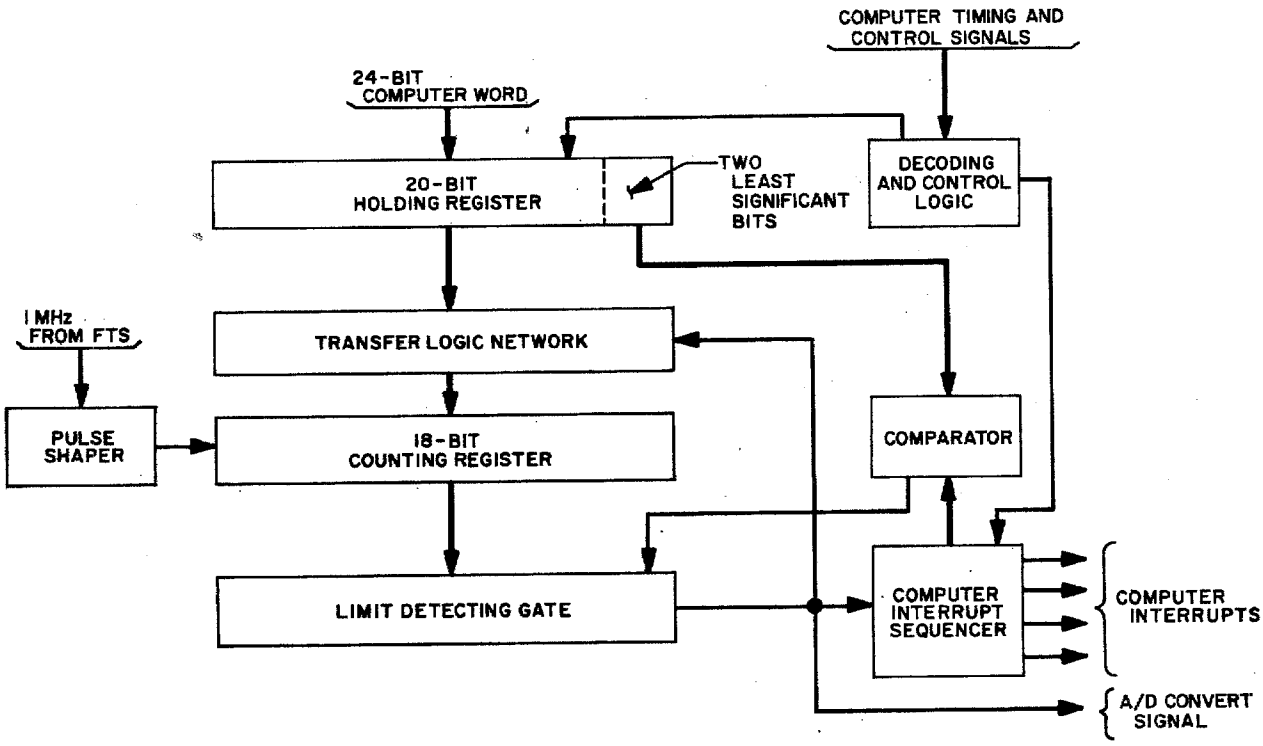


Fig. 56. Digital phase shifter/timing generator block diagram

Since this operation is continuous and cyclic, the limit detecting gate is true and generates an output to the timing generator portion once every $T_b/4$. The holding register is accessed directly by the computer program via an energize output M (*EOM*) 3 instruction, and a value placed in the register by a following parallel output (POT) instruction from the computer word bits 4 through 23. Since this value is the result of computation by the timing algorithm, and the contents of the holding register can be modified at will by the program, phase shifting of the timing signals can be accomplished by increasing or decreasing, for a given number of $T_b/4$ periods, the value held in the register, and consequently the number of microsecond pulses counted by the counting register. Since varying this count is equivalent to an apparent change in the duration of $T_b/4$, a phase shift of the timing pulse is accomplished.

The timing generator consists of a scale-of-four divider chain which uses the limit detecting gate signal to generate computer interrupts (i.e., the timing signals) and to sequence them in the proper order. In addition, a *convert* signal is generated at each $T_b/4$ time and is sent to the A/DC. This ensures that the incoming data bit stream is sampled coherently with the bit transition time.

In order to obtain the resolution of the basic clock frequency (1 MHz) over the entire bit duration, a comparator circuit is used between the two least significant bits of the holding register and the timing generator divider chain. The holding register has a capacity of two more bits at the least significant end than has the counting register. If these two bits, which are the two least significant bits of the value computed by the timing algorithm, are considered as a number H, ranging from 0 to 3, and if the timing generator divider chain bits are similarly considered a number T, then by comparing H and T such that if $H > T$ the counting register is allowed to count one additional microsecond each $T_b/4$, a total resolution of 1 μs is achieved over the entire bit duration. The size of the counting register permits a total range of bit rates from less than 1 to 10^6 bits/s with the resolution of 1 μs, as described above.

Further control circuitry in the phase shifter/timing generator performs such tasks as EOM decoding, clocking the POT and interrupt signals with the correct computer clock phase or control signals, and shaping of the 1-MHz frequency standard from the frequency and timing subsystem (FTS), for use as the internal clocking and timing signal.

Implementation. The digital phase shifter/timing generator is to be implemented completely with Division 33 standard Hi-Rel digital modules. The complete system will be mounted in a drawer-type card cage and, together with the necessary power supplies, installed in the data conversion equipment rack as part of the TCP-IIC modifications.

Interface signals with the phase shifter will be via the standard computer POT connector, which carries all the necessary control signals as well as the computer word bits. The timing generator will interface via RG-55 cables terminated in TNC connections as will the 1-MHz standard frequency from the FTS.

There are no control devices, e.g., push buttons or switches, associated with this equipment, since in its final configuration it is completely under computer control in its operation.

Multiplexers. The multiplexers accept AGC and SPE from both receivers and integrated data streams from both subcarrier demodulators. Each input is assigned to its corresponding multiplexer input channel. The multiplexers operate under computer program control with the computer selecting the required channel to be sampled. Other features of the multiplexers include:

(1) Full-scale input voltage of ± 5 V.

(2) Input impedance of 10K.

(3) 16 differential input channels.

(4) Sample rate of 50,000 samples/s.

(5) Channel selection by random binary address.

Analog-to-digital converters. Analog output voltages of the multiplexers, such as receiver AGC, SPE or integrated data stream are input to the analog-to-digital converters. Two analog-to-digital converters are used and operate in the following manner: (1) One analog-to-digital converter samples input voltages of receiver AGC and SPE. Conversion to digital data is initiated automatically after the proper multiplexer input channel has been selected by the computer program, and (2) a second analog-to-digital converter samples the integrated data stream input from the subcarrier demodulator assembly. Conversion is initiated by timing signals from the digital phase shifter/timing generator. Characteristic features of the analog-to-digital converters include:

(1) Conversion time of 1.5 μs/bit.

(2) Output resolution consists of 11 binary magnitude bits plus sign with *two's* complement for negative numbers.

(3) Conversion accuracy of 0.025% of full-scale value (± 5 V).

(4) Sample and hold capability.

Communication buffer. The primary function of the communication buffer is to transmit computer detected and formatted data bit stream to SFOF via teletype send circuits and high-speed data line (HSDL). A communication buffer is provided with each computer assembly (Alpha and Beta) and communication with the computer is via the computer parallel input/output channel. Each communication buffer consists of the following units.

Teletype Communication Equipment. Three full duplex teletype communications channels each capable of simultaneously transmitting and receiving are provided for the Alpha and Beta assemblies. These teletype channels interface with common carrier transmission lines for communications with the SFOF. Telemetry data are transmitted in standard Baudot Code (five information bits per character) at a rate compatible with the teletype terminal equipment at each station. The standard rates are presently 60 or 66.7 words/min. A communications patch panel allows send and receive channels to be connected to selected teletype lines.

HSDL Register. The HSDL register transmits computer data to SFOF via the NASCOM system. Preamble data required by the NASCOM system and formatted bit information are presented to the register via the computer parallel output channel for conversion to a serial bit data. The register serial output bit stream is transmitted to the HSDL modem of the DSIF GCS in synchronism with clock pulses supplied by the modem. The HSDL register is capable of operating at data rates of 660, 1200 or 2400 bits/s synchronous with an external timing source.

3. Demonstration Software, *J. W. Layland*

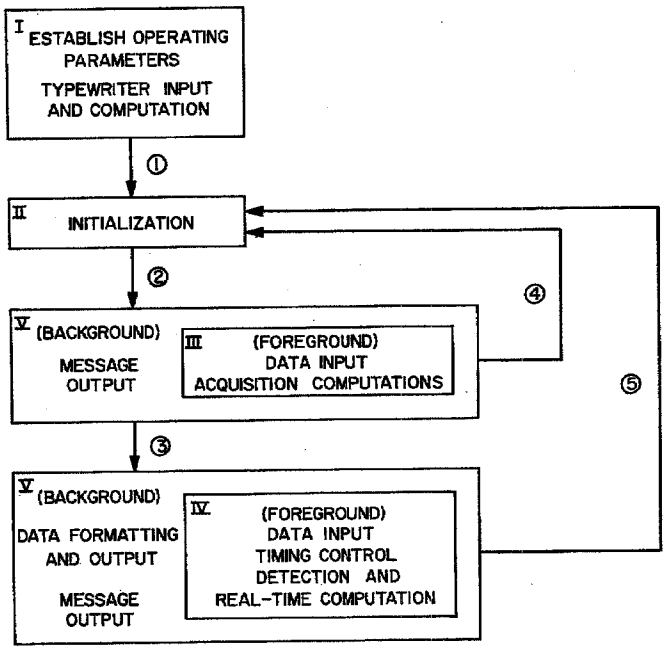
A glance at Fig. 1 reveals one important fact about the MMTS: that the SDS 920 computer and its controlling program have become an integral part of the demodulator. In order to perform the system verification tests, some form of the mission-independent software must be coupled with enough output software that the entire system's performance may be observed. This is the primary purpose of the demonstration software. Of nearly equal importance is the intent that the control/detection segments of

the demonstration software serve as a prototype for the mission-independent segments of future software. Associated with these two purposes are the (possibly) conflicting requirements that the control/detection segments be as close to optimal as possible, and that the software package adapt easily to modification in hardware parameters. The succeeding paragraphs describe the specific requirements on the demonstration software and the details of its implementation, particularly of the control/detection (or mission-independent) segments.

The requirements on the demonstration software are most readily describable in terms of the available inputs and required outputs from the software. The outputs required are: (1) the detected data stream, (2) an estimate of signal-to-noise ratio, (3) information of the in-lock status of the RF and subcarrier tracking loops. These must be recorded on magnetic tape as the prime data record, and formatted for other appropriate output. In addition, the program must compute and type the bit-error rate when the data source is the MMTS test equipment.

During real-time operation, the software inputs consist of: (1) the timing marks (interrupts) from the program-controlled timing generator, (2) the sampled and digital value of the MMTS integrator, (3) the status (in-lock/out-of-lock) of the RF and subcarrier phase-locked loops, (4) the transmitted data bits (when input is from the test equipment). A necessary condition for the performance of this input/output processing is that the timing generator be synchronized to, and kept in close synchronism with, the transitions of the received data stream. To minimize loss of data in acquisition, it is desirable that the initial synchronization be done as fast as possible. The program must run "comfortably" at bit rates of up to 512 bits/s.

The demonstration software package being written to satisfy these requirements is a direct descendent of both the audio model software (Sect. D) and the type III demonstration software (SPS 37-45, Vol. III, pp. 51–57). The package is divided into six major blocks (Fig. 57). Block I, entered when the program is loaded and reenterable at cell 0240, accepts four parameters from the console typewriter: (1) bit rate, (2) integration time constant, (3) nominal signal-to-noise ratio, and (4) loop bandwidth of the bit-time tracking loop. It then computes thresholds, gain constants, and scaling instructions and sets these for use in and by the real-time processing blocks. Most computations in this block are performed in floating-point mode. Most of the computations performed here would be unnecessary in an operating system where bit



TRANSITIONS OCCUR AS FOLLOWS:
① UNCONDITIONALLY
② RF AND SUBCARRIER LOOPS SECURELY LOCKED
③ ACQUISITION DATA SATISFACTORY
④ RF OR SUBCARRIER LOOP OUT-OF-LOCK OR ACQUISITION DATA NOT SATISFACTORY
⑤ RF, SUBCARRIER, OR BIT SYNC LOOP CONSISTENTLY OUT OF LOCK

Fig. 57. Demonstration program block

rate, and other parameters linked to it, would be selected from a finite set. When this computation is completed, control is transferred to Block 2, which initializes buffer pointers and flags, conditions the interrupts, and links the initializing interrupt routines of Block 3 to the proper points. When the RF and subcarrier loops have reached a stable in-lock condition, the interrupts are enabled and control transferred to the non–real-time data processing in Block 5. Block 2 may be reentered manually from cell 01, or from a *bad data* condition in the non–real-time data processor. Blocks 3 and 4 comprise the real-time data processor and will be given a complete description shortly. The non–real-time data processor, Block 5, performs all of the output formatting, data validation, bit-error rate computation, etc., in response to flags set by the interrupt routines in Block 4, using data supplied by the interrupt routines on a set of circular cues. Twenty-four received data bits comprise one word of the data cue, while the sum-of-absolute-values and sum-of-squares of the data-integrals of these 24 bits and the number of subcarrier and RF loop *not-locked* responses associated with these bits are entered on parallel cues. Figure 58 is a skeletal

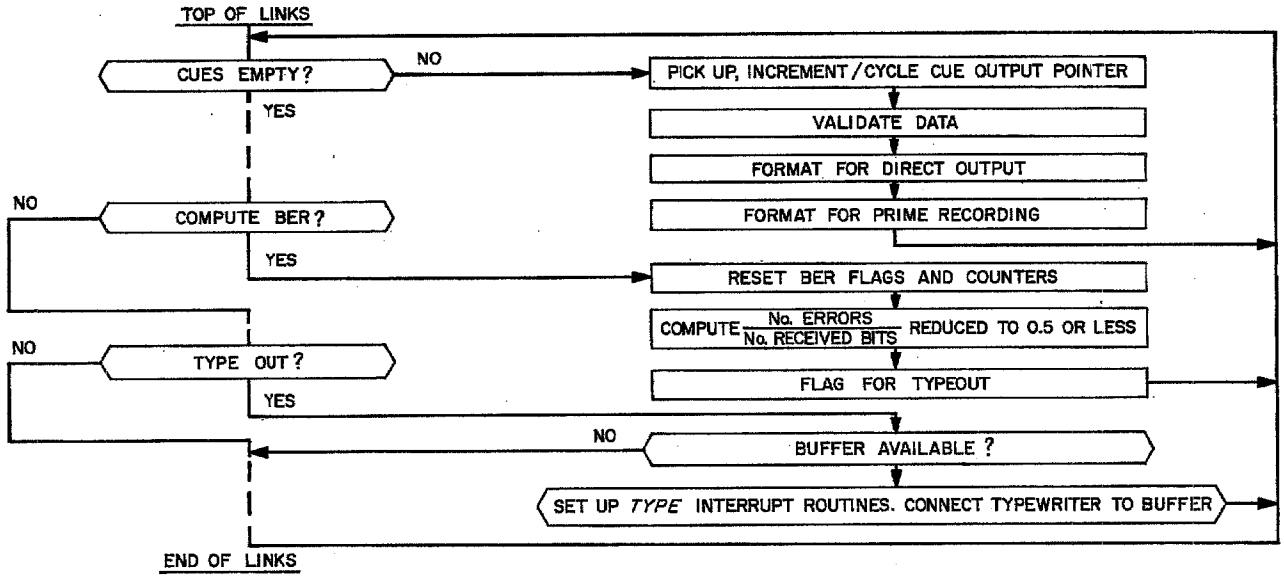


Fig. 58. Block 5 flow diagram

flow diagram of Block 5. The dashed lines represent other processor options which are not shown explicitly, but which are handled similarly to those shown. The *validate-data* routine performs some of the important mission-independent functions and will be described fully later. Block 6 contains storage locations, cues, and data buffers. When the program assumes final form, Block 6 will also be a dictionary of all labels used in the program.

Figure 59 is a flow diagram of the Block 4 real-time processing routines. Subroutine *erlytrk* responds to an interrupt signal occurring ¼-bit time before the data transition time. Subroutine *datatrk* responds to an interrupt signal at the data transition time, while the interrupt signal which energizes *latetrk* occurs ¼-bit time after the data transition time. The basic cost (in machine time) of these routines is 142 cycles for each cycle through the trio (once per bit time). To this must be added an incremental load of 43 cycles for placing the packed data on the cues, an overhead of 21 cycles if the bit-error-rate option is selected, and a scaling cost which may vary from 0 to 13 cycles, depending upon the signal level at the A/D input. Of the basic cost, 37 cycles are spent storing data samples and handling the interrupt routine entry and exit, 32 cycles to compute the timing-error sample, 20 cycles to filter this sample (a double-integrator filter is used) and update the time generator, and 36 cycles to compute the data integral, detect the data bit, and update the sum-of-absolute values and sum-of-squares used in estimating SNR. The remaining time is consumed by performing brief bookkeeping.

If the data stream is at 512 bits/s, there are nominally 244 computer cycles available per bit. To sustain operation, neither the peak level of real-time processing during a given received bit nor the overall average processing cost may exceed this. With scaling taking its maximum load of 13 cycles and the bit-error-rate option active, the peak load is 219 cycles. There may, in addition, be one (and only one) typewriter/buffer interrupt of higher priority than the timing generator which will insert a 12- or 13-cycle overload, bringing possible peak consumption to 232 cycles, quite close to the limit. Since only token typewriter output is required with this option, the average constraint is of no consequence.

Without using the bit-error-rate option, the peak load of the Block 4 routines is reduced to 198 cycles; but the typewriter may again contribute 13 cycles, and an interlaced magnetic tape may require 12 cycles stolen by the interlace for memory access plus a minimum of 7 cycles for an end-of-record interrupt, bringing the peak load total to 230 cycles. It has been assumed (and is probably necessary) that the comm-buffer interrupts be of lower priority than those of the timing generator, thus removing them from this critical timing consideration. Noninterruptable sequences of more than 10 cycles' duration must be avoided in the non–real-time processor to allow reasonable assurance that the complete package will run. In particular, this eliminates the divide instruction and shifts of more than 16 places. The average cost per bit is a more reasonable 157 cycles in the data transfer mode, leaving a nominal 77 cycles per data bit available for formatting

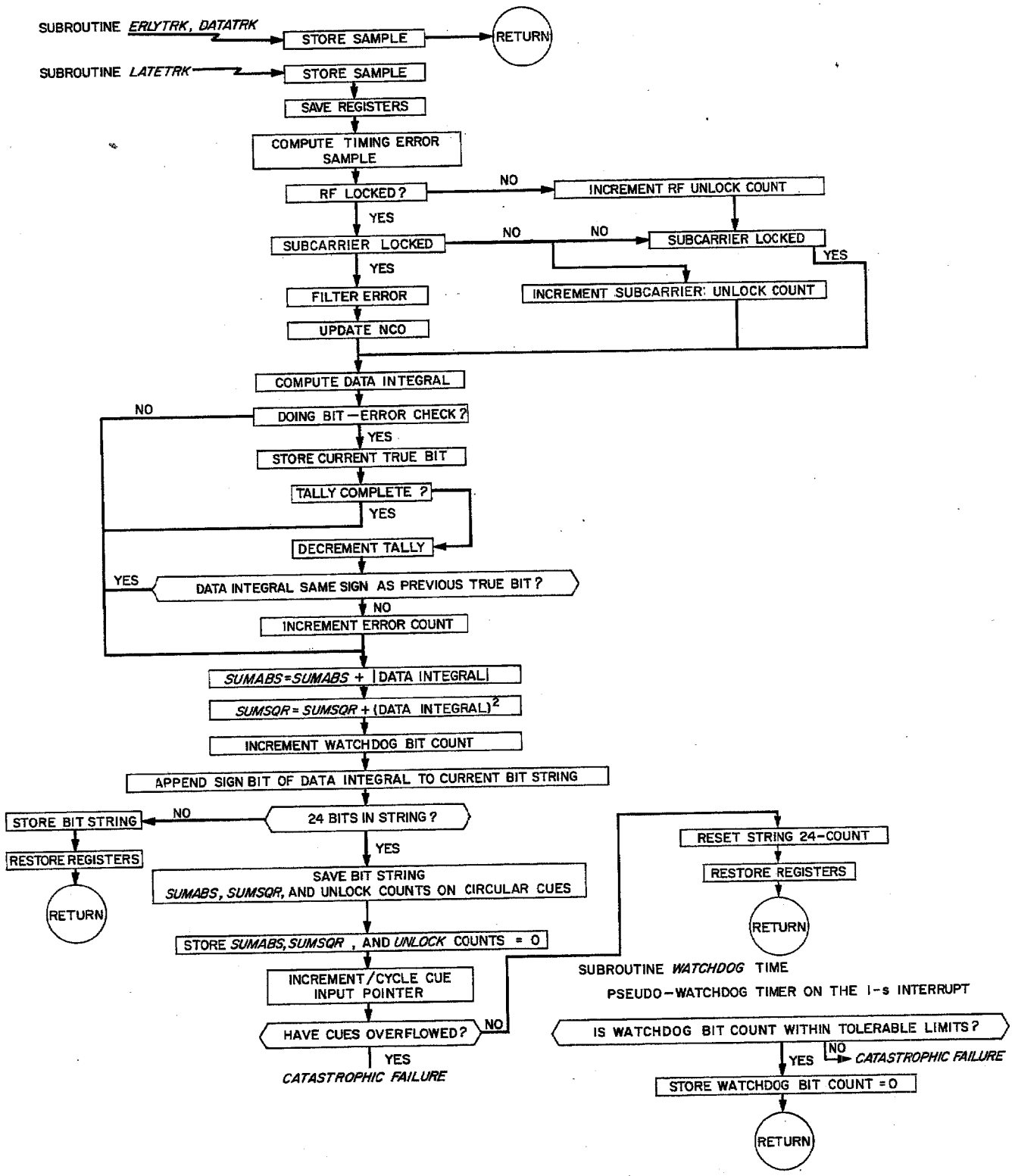


Fig. 59. Block 4 real-time data-processing routines

and output processing. While this figure could never be reached in practice, most of it should be available if the cyclical cues are made long enough to average over the periodic work load for the non–real-time data processing.

Block 3 contains the acquisition and transition real-time processing routines. There are three distinct sub-blocks or phases to this block of routines. The first phase initializes linkages and constants for the second phase and guarantees that this second phase is initiated at the proper point in the timing generator interrupt cycle. The third phase performs this same task for the Block 4 routines, in addition to shifting the timing generator into synchronism with the data-bit transition. Figure 60 is a flow diagram of the second phase, which computes the delay between the data interrupt signal of the timing generator and the received data transitions. *Quatarun* is alerted by an interrupt signal at the mid-bit or data-quadrature time of

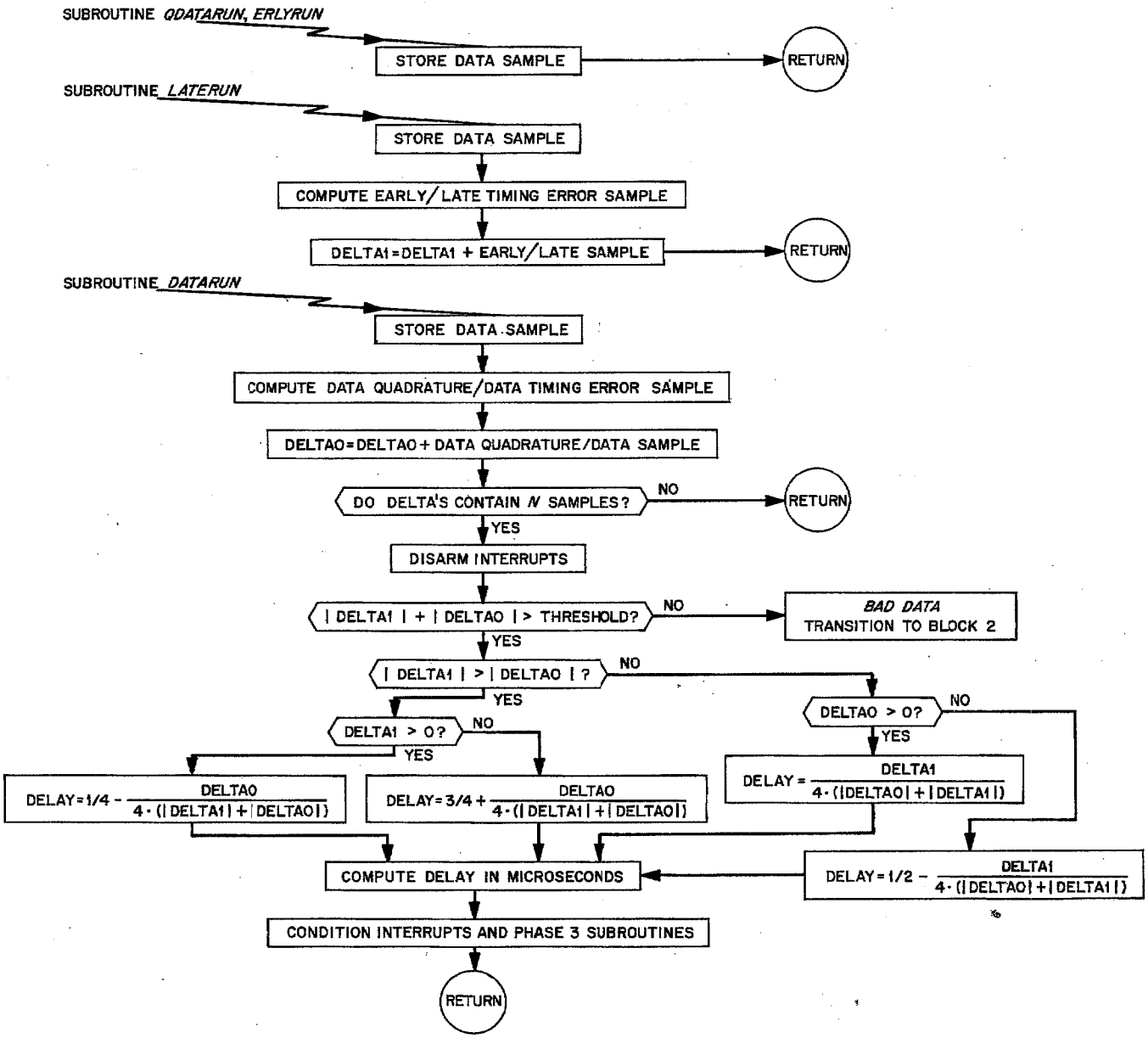


Fig. 60. Block 3, sub-block 2, real-time acquisition routines

the timing generator. The other routines are activated by the interrupt signal which activates their Block 4 counterpart as already described. Computation of "Delta0" and "Delta1," the total real-time load, takes 156 cycles per data bit—well within the 244 cycles available at 512 bits/sec. The final computation of the delay shift takes place with interrupts disarmed and hence does not contribute to the real-time load. In addition to those routines already described, an interrupt routine operating at a 1-ms request rate interrogates the RF and subcarrier lock indicators. If a persistent out-of-lock condition is found at any time during the Block 3 processing, acquisition is aborted and control is transferred to Block 2.

Subroutine *locktest* performs the data validation functions in the non–real-time data processor. Its flow diagram is shown in Fig. 61. The SNR estimated from the sum-of-absolute values and sum-of-squares of the data integrals for the current 24 bits is used as a lock indicator for the overall system. The RF and subcarrier loops are considered to be out-of-lock if the number of *not locked* responses during detection of these 24 bits exceeds a preset threshold. Any *not locked* condition which is sufficiently persistent to invalidate the bit-timing system status will cause a transfer to Block 2, an appropriate message, and a subsequent reacquisition.

4. MMTS Test Equipment, *R. G. Petrie*

a. General requirements. A necessary adjunct to any major system development is the special test equipment required to establish and maintain the correct operation of the system. The MMTS is such a system for which special test equipment is needed. The general requirements for the test equipment are as follows:

Baseband output signal. A test signal comprised of a bit stream, with or without superimposed noise, to be used for testing the digital portion of the MMTS only.

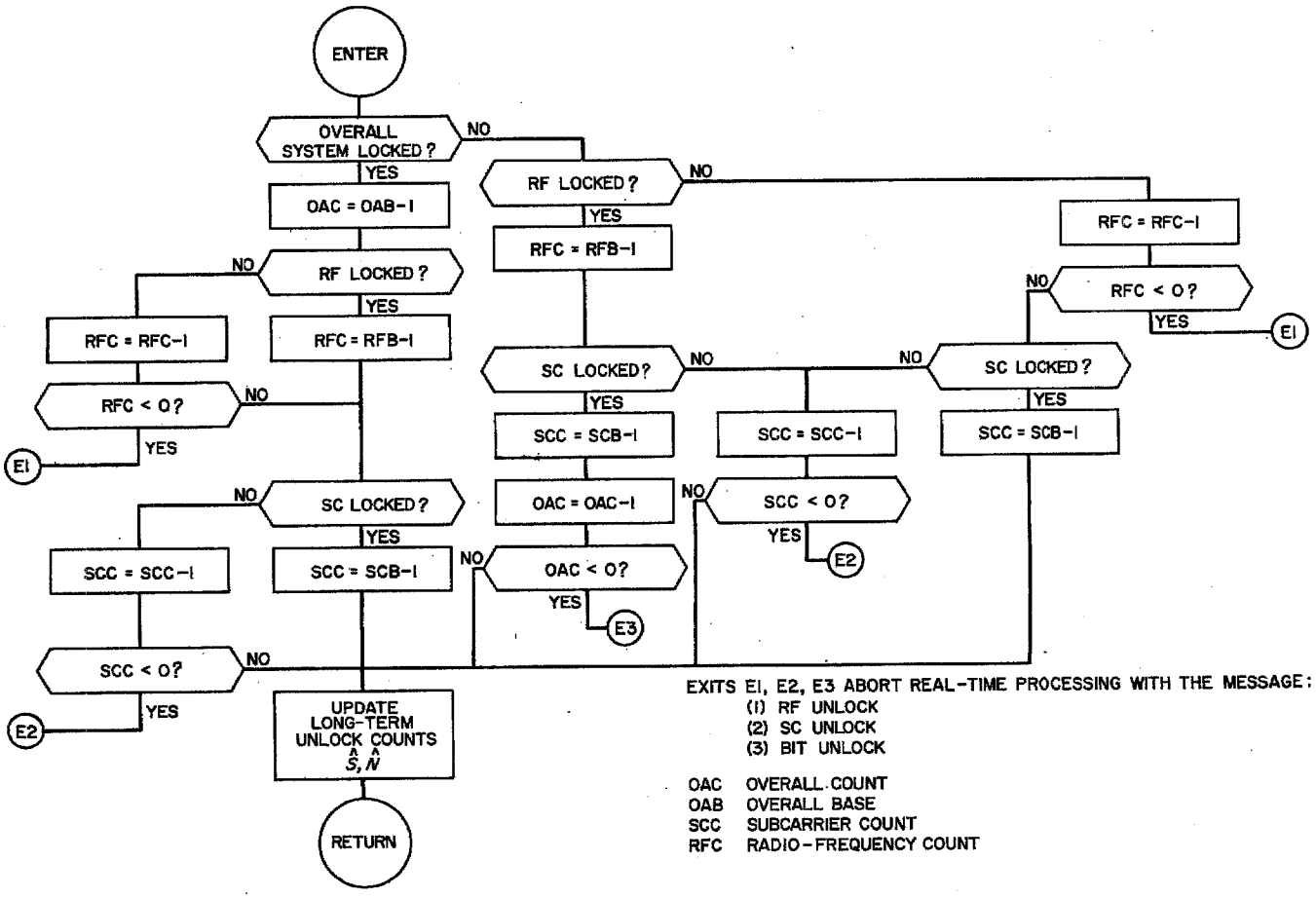


Fig. 61. Subroutine *locktest* flow diagram

Subcarrier output signal. A test signal comprised of a subcarrier, modulated with a bit stream, with or without superimposed noise, to be used for testing the entire MMTS.

Carrier output signal. A test signal comprised of a subcarrier, modulated with a bit stream, to be in conjunction with the test transmitter to modulate an S-band carrier for testing the combined MMTS and S-band receiver system.

Bit-error checking. A method whereby the data stream bits as generated by the test equipment are compared, bit by bit, with the data bits recovered by the MMTS and an error tally or bit error rate computed and displayed.

Simulation input. Provisions are made for external data sources, such as magnetic tape recordings of simulated or actual spacecraft data, to be used in place of the internal bit stream generator.

Test flexibility. The test equipment should be sufficiently versatile to allow tests closely simulating actual operating conditions. Thus, the test equipment should be able to supply, for instance, two subcarriers, each modulated with data, to test the ability of the MMTS subcarrier demodulator to reject the unwanted subcarrier and recover the desired data.

The various test signals and their entry points in the station equipment assemblies are shown in Fig. 3.

b. Equipment description and operating modes. Figure 2 shows a complete block diagram of the MMTS test equipment. This block diagram is referenced in the following description.

Signal sources. Two subcarrier oscillators are shown on the block diagram. Oscillator 1 is the primary oscillator for generating the desired subcarrier frequency and is a precision oscillator of the synthesizer type. Oscillator 2 can be used to generate a second subcarrier frequency when desired, but its primary purpose is to provide a clock frequency at the desired data bit rate. This oscillator is not as precise as oscillator 1, being only a high-quality L-C type oscillator rather than a synthesizer, and consequently should not be used as the main subcarrier generator.

Both subcarrier outputs are converted into square waves by means of the shaper circuits indicated on the block diagram.

The bit-stream generator is a multifunction device having the following capabilities:

(1) A pseudo-noise (PN) sequence of equally probable *ones* and *zeros*. Several different length PN sequences will be available to the operator through proper setting of a pair of selector switches.

(2) A square wave, i.e., an alternating series of *ones* and *zeros*.

(3) A constant stream of either *ones* or *zeros* into which can be inserted a single bit of opposite polarity at the discretion of the operator. This function is desirable in testing the recovery capability of the integrators in the subcarrier demodulation loop.

When in use, the bit stream generator uses subcarrier oscillator 2, which is set at the data bit rate, as a clock pulse generator.

Two additional signal sources are available through use of the external data source inputs 1 and 2, as shown on the block diagram. These inputs would be used if, for example, it is required to have two simultaneous and independent data streams or if two simultaneous subcarrier frequencies are desired. These inputs provide the simulation input capability described above in the list of general requirements.

These various signal sources can then be combined and processed in the following ways:

Signal conditioning and output. A direct output of the data bit stream is provided at the bit-error check outputs 1 and 2. These outputs are used by the computer in determining the bit-error rate and, in normal test configurations, they are reserved exclusively for this use.

The data stream outputs 1 and 2 are used for the baseband testing capability as stated in the general requirements above. Provision is made to allow the operator to first mix noise with the bit stream, if desired, using the precision signal-to-noise mixer available at each DSS station. The signal is next processed through an integrator identical to the one shown in the output of the subcarrier demodulation loop on the MMTS block diagram. This integrator has five switch-selected decade time constants to cover the range of bit rates required. Finally, the signal is processed through a variable gain isolation amplifier for level adjustments and impedance matching.

The test signal available at the data plus subcarrier output is comprised of one or both subcarrier frequencies,

each of which is modulated with a data bit stream and with or without superimposed noise. To achieve this configuration, each subcarrier is first combined with its data stream in a modulator. Since both the subcarrier and the bit stream are square waves, and the desired modulation is biphase, the modulator consists of an *exclusive or* gate or a modulo two adder. The action of this modulator can best be seen by noting the truth table for an *exclusive or* function:

Subcarrier	Data	Modulated output
0	0	0
0	1	1
1	0	1
1	1	0

Note that a "0" can be considered zero or reference phase and a "1" can be considered 180-deg phase in the above table.

The modulated subcarriers are then passed through a precision attenuator for level setting and are summed in a fixed gain isolation amplifier. The output of this amplifier can be switched through the precision signal-to-noise mixer depending upon the use of the test signal at this point. By referring to Fig. 3, it can be seen that the test signal sent to the test transmitter and that sent to the input of the MMTS subcarrier demodulator differ only in the absence or presence of noise, respectively. Either signal can thus be generated by the same modules in the test equipment.

The previous section has described the operation of the test equipment insofar as the generation of the

Table 8. Test equipment operating modes

Mode of operation	Function			Outputs	System entry point (Fig. 1)
	Subcarrier oscillator 1	Subcarrier oscillator 2	Data bit-stream source		
Test					
Baseband single channel	Not used	Data bit-rate clock	Bit stream generator	Data stream output 1	Input to MMT bit synchronizer
Subcarrier single channel	Subcarrier frequency generator	Data bit-rate clock	Bit stream generator	Data + subcarrier with noise	Input to MMT subcarrier demodulator
Carrier	Subcarrier frequency generator	Data bit-rate clock	Bit stream generator	Data + subcarrier	Input to test transmitter
Simulation					
Baseband single channel	Not used	Not used	External data source No. 1	Data stream output 1	Input to MMT bit synchronizer
Baseband dual channel (primary)	Not used	Not used	External data sources 1 and 2	Data stream outputs 1 and 2	Input to MMT bit synchronizer
Baseband dual channel (secondary)	Not used	Data bit-rate clock	Bit stream generator and external data source 2	Data stream outputs 1 and 2	Input to MMT bit synchronizer
Subcarrier single frequency	Subcarrier frequency generator	Not used	External data source 1	Data + subcarrier with noise	Input to MMT subcarrier demodulator
Subcarrier dual frequency	Subcarrier 1 frequency generator	Subcarrier 2 frequency generator	External data sources 1 and 2	Data + subcarrier with noise	Input to MMT subcarrier demodulator
Carrier, single subcarrier frequency (primary)	Subcarrier frequency generator	Not used	External data source 1	Data + subcarrier	Input to test transmitter
Carrier, single subcarrier frequency (secondary)	Subcarrier frequency generator	Data bit-rate clock	Bit stream generator	Data + subcarrier	Input to test transmitter
Carrier, dual subcarrier frequency	Subcarrier 1 frequency generator	Subcarrier 2 frequency generator	External data sources 1 and 2	Data + subcarrier	Input to test transmitter

In all cases, the appropriate bit-error check outputs are used for the bit error rate computation.

required test signals. Additional details not directly connected with the signal generation will be covered in the section on implementation that follows.

Operating modes. The MMTS test equipment has two basic roles to fulfill: (1) to provide a testing and troubleshooting capability for the MMTS, and (2) to aid in simulation and training. While both of these functions are similar, they have distinct differences in the test equipment configurations required to support them. The several operating modes, both test and simulation, are presented in Table 8.

c. Implementation. In addition to the equipment description above, the following implementation details are presented to further describe the MMTS test equipment configuration.

The bit-error rate computation, referred to in the above discussion, will not be implemented through hardware but will instead be a program routine entered in the TCP computer during the time testing or simulation is being done. The bit-error check outputs are directly connected to the computer for this purpose. Display of the bit-error rate computation results will be via the computer console typewriter.

All of the signal switching required to generate specific test signals will be done on a semiautomatic basis. A specific mode setup will require only one action on the part of the operator, exclusive of attenuator or data format control settings.

An oscilloscope, permanently mounted in the test equipment rack, is used to monitor the various signals being generated. Test points will be brought to a central control and patch panel, thus permitting the operator to locate quickly any problems that may arise in the test equipment itself.

The bit-stream generator will be constructed of JPL Division 33 Hi-Rel standard digital modules with the necessary selecting controls brought out to the central control panel.

All the isolation amplifiers and the integrators shown on the block diagram will be operational amplifiers appropriately connected. There are isolation amplifiers in addition to those actually shown on the block diagram, but they are primarily of a fixed impedance and gain matching function and consequently are not included in the functional diagram.

The entire test equipment is to be mounted in a roll-around standard DSIF equipment rack with all connectors and cables necessary to perform its functions. The test equipment rack is to be complete in itself with no need for auxiliary test devices, except the precision signal-to-noise mixer. Each station that is equipped with the MMTS (either single or dual channel) will be provided with one set of MMTS test equipment.

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